F I G. 1

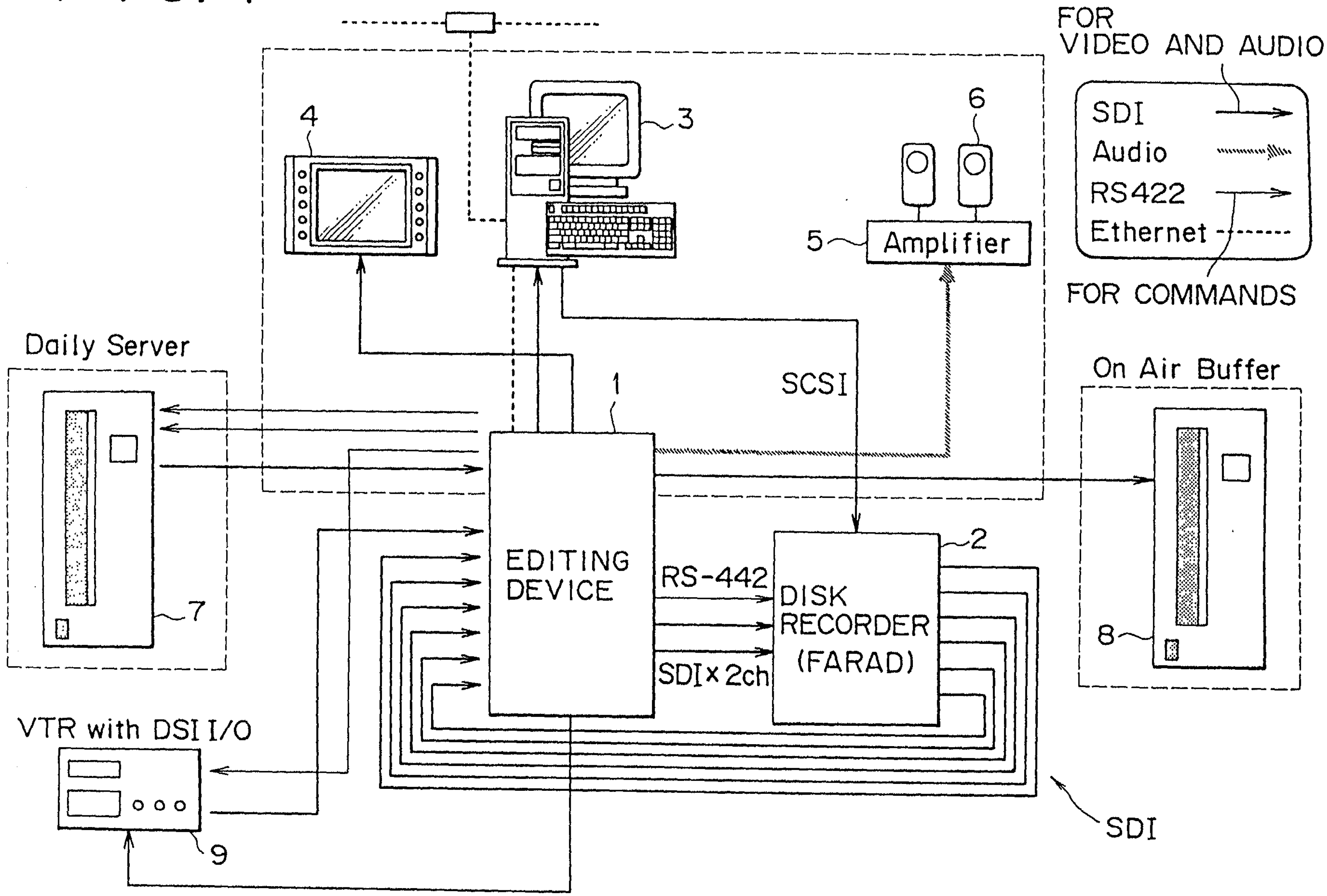
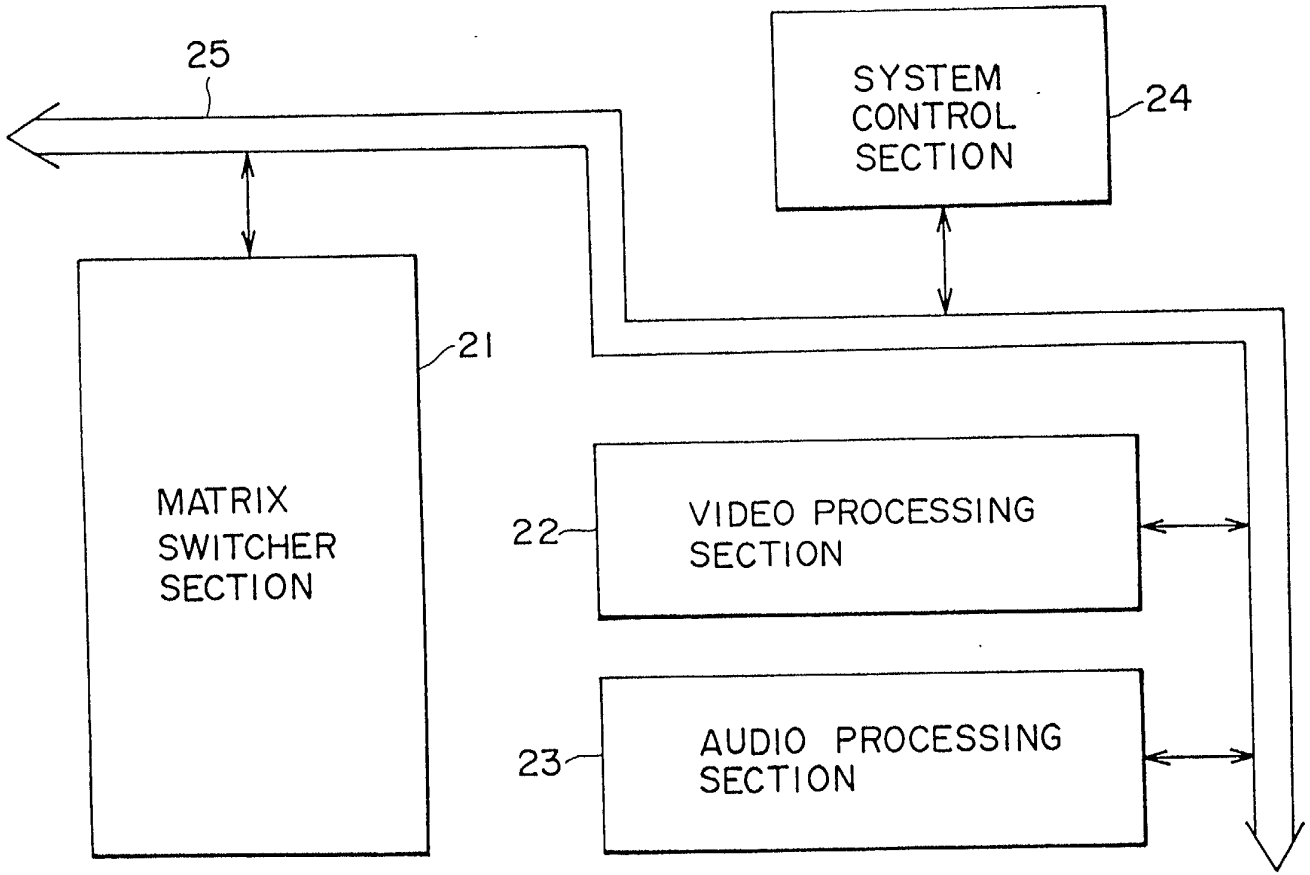
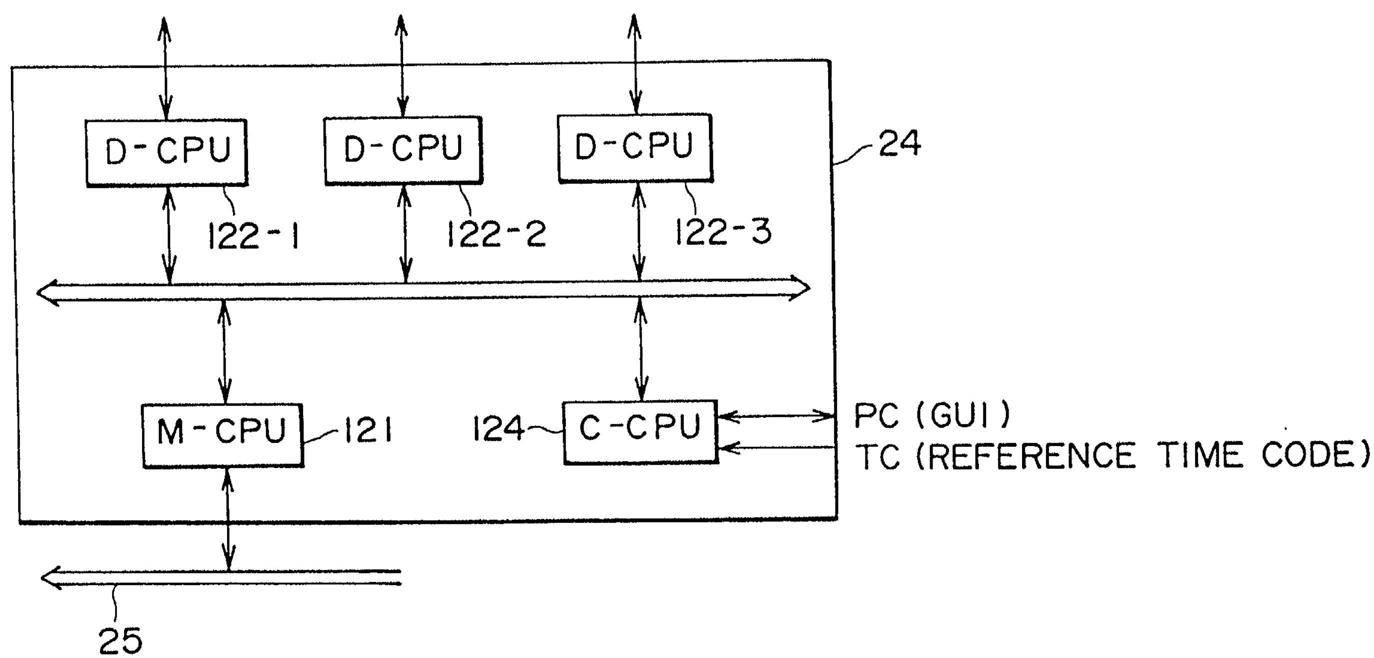

FOR
VIDEO AND AUDIO
SDI
Audio
RS422
Ethernet
FOR COMMANDS
Daily Server
7
4
3
6
5
Amplifier
1
SCSI
On Air Buffer
8
EDITING
DEVICE
RS-442
SDI x 2ch
DISK
RECORDER
(FARAD)
2
VTR with DSI I/O
9
SDI

FIG.2

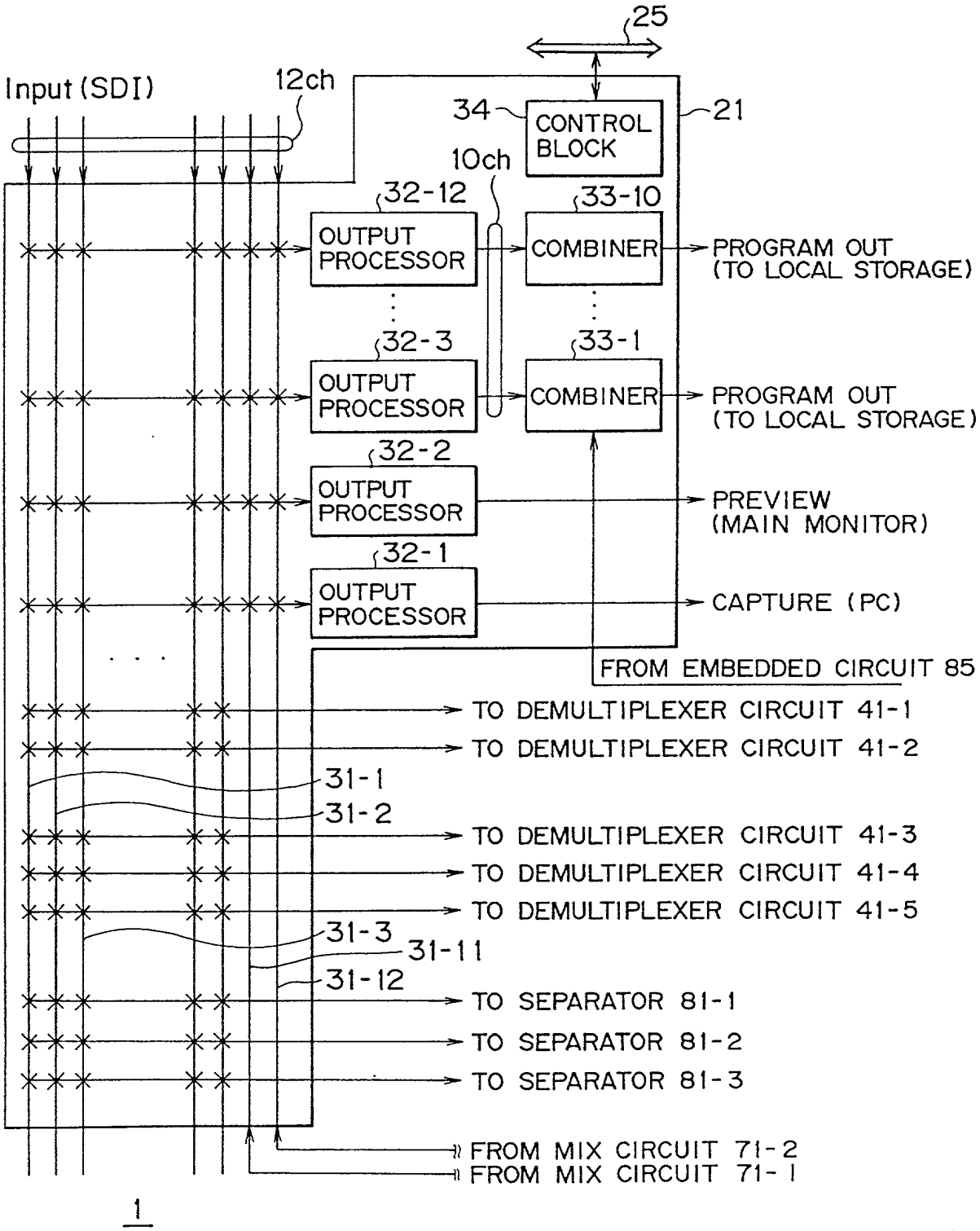


F I G. 3



D-CPU
D-CPU
D-CPU
24
122-1
122-2
122-3
M-CPU
121
124
C-CPU
PC (GUI)
TC (REFERENCE TIME CODE)
25

FIG. 4


25
Input (SDI)
12ch
34
CONTROL BLOCK
21
10ch
32-12
OUTPUT PROCESSOR
33-10
COMBINER
PROGRAM OUT (TO LOCAL STORAGE)
32-3
OUTPUT PROCESSOR
33-1
COMBINER
PROGRAM OUT (TO LOCAL STORAGE)
32-2
OUTPUT PROCESSOR
PREVIEW (MAIN MONITOR)
32-1
OUTPUT PROCESSOR
CAPTURE (PC)
FROM EMBEDDED CIRCUIT 85
TO DEMULTIPLEXER CIRCUIT 41-1
TO DEMULTIPLEXER CIRCUIT 41-2
31-1
31-2
TO DEMULTIPLEXER CIRCUIT 41-3
TO DEMULTIPLEXER CIRCUIT 41-4
TO DEMULTIPLEXER CIRCUIT 41-5
31-3
31-11
31-12
TO SEPARATOR 81-1
TO SEPARATOR 81-2
TO SEPARATOR 81-3
FROM MIX CIRCUIT 71-2
FROM MIX CIRCUIT 71-1

1

FIG. 5

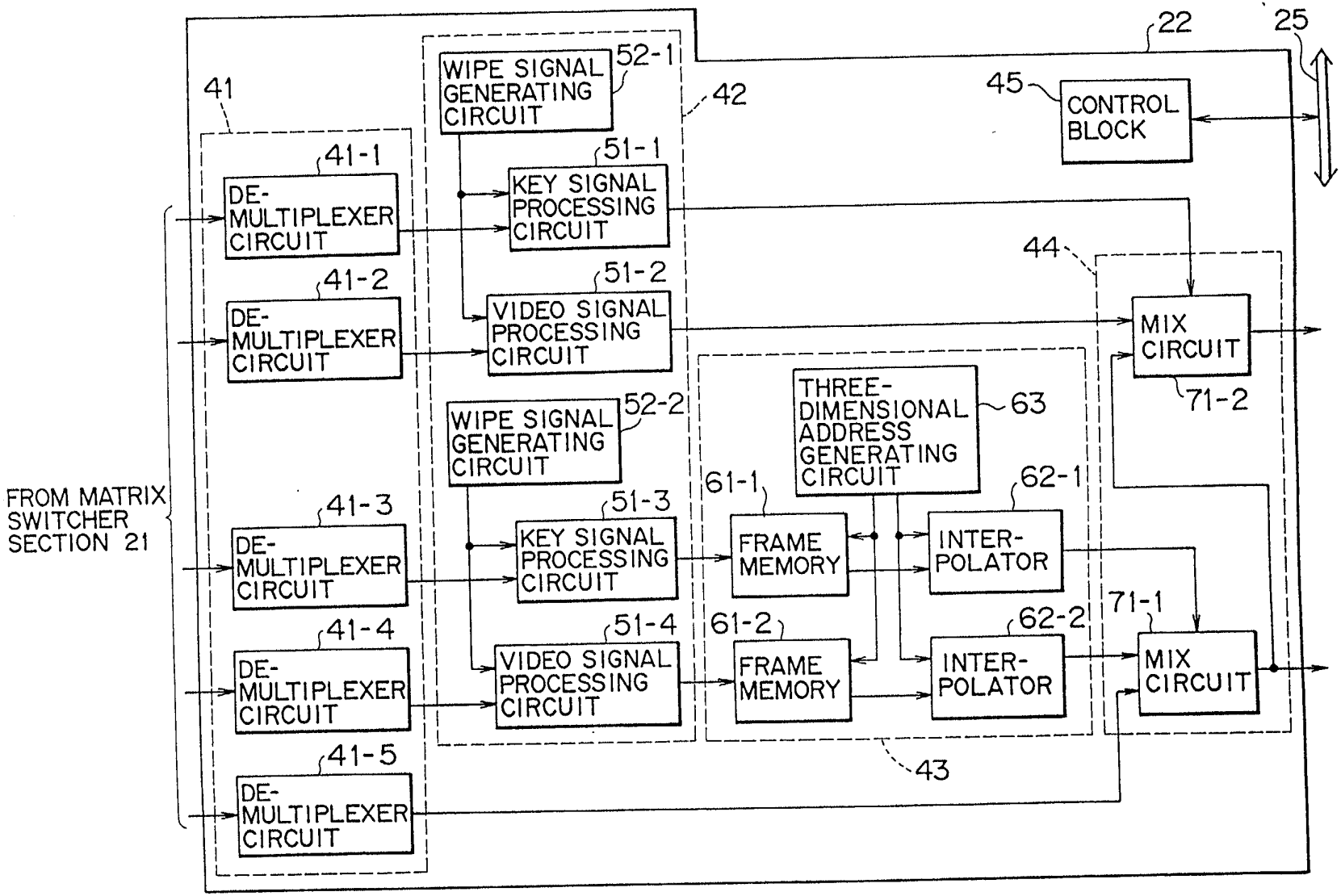


FIG. 6

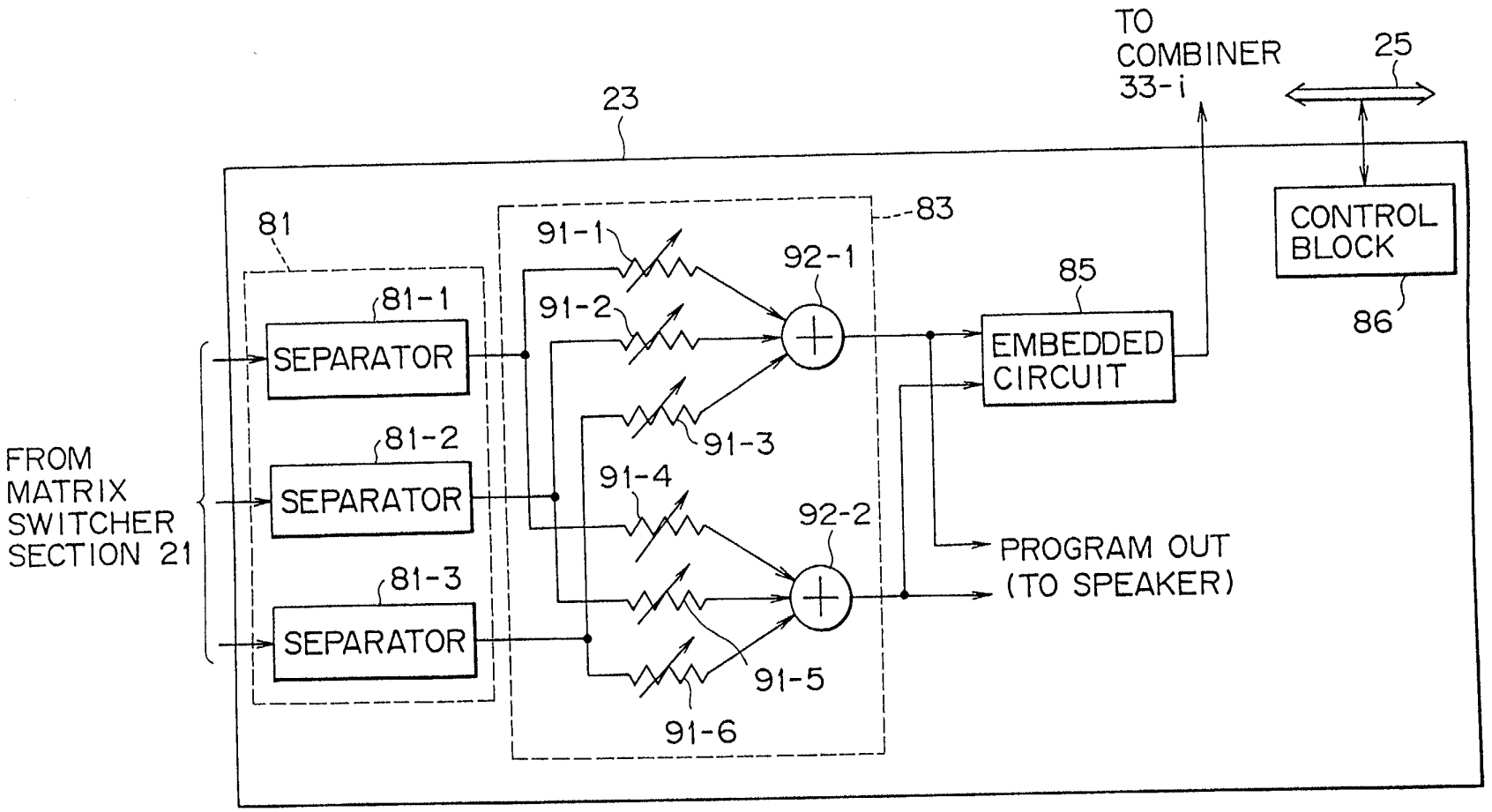

TO
COMBINER
33-i
25
23
CONTROL
BLOCK
86
81
83
91-1
92-1
85
81-1
91-2
SEPARATOR
EMBEDDED
CIRCUIT
91-3
FROM
MATRIX
SWITCHER
SECTION 21
81-2
91-4
92-2
SEPARATOR
PROGRAM OUT
(TO SPEAKER)
81-3
SEPARATOR
91-5
91-6

FIG. 7

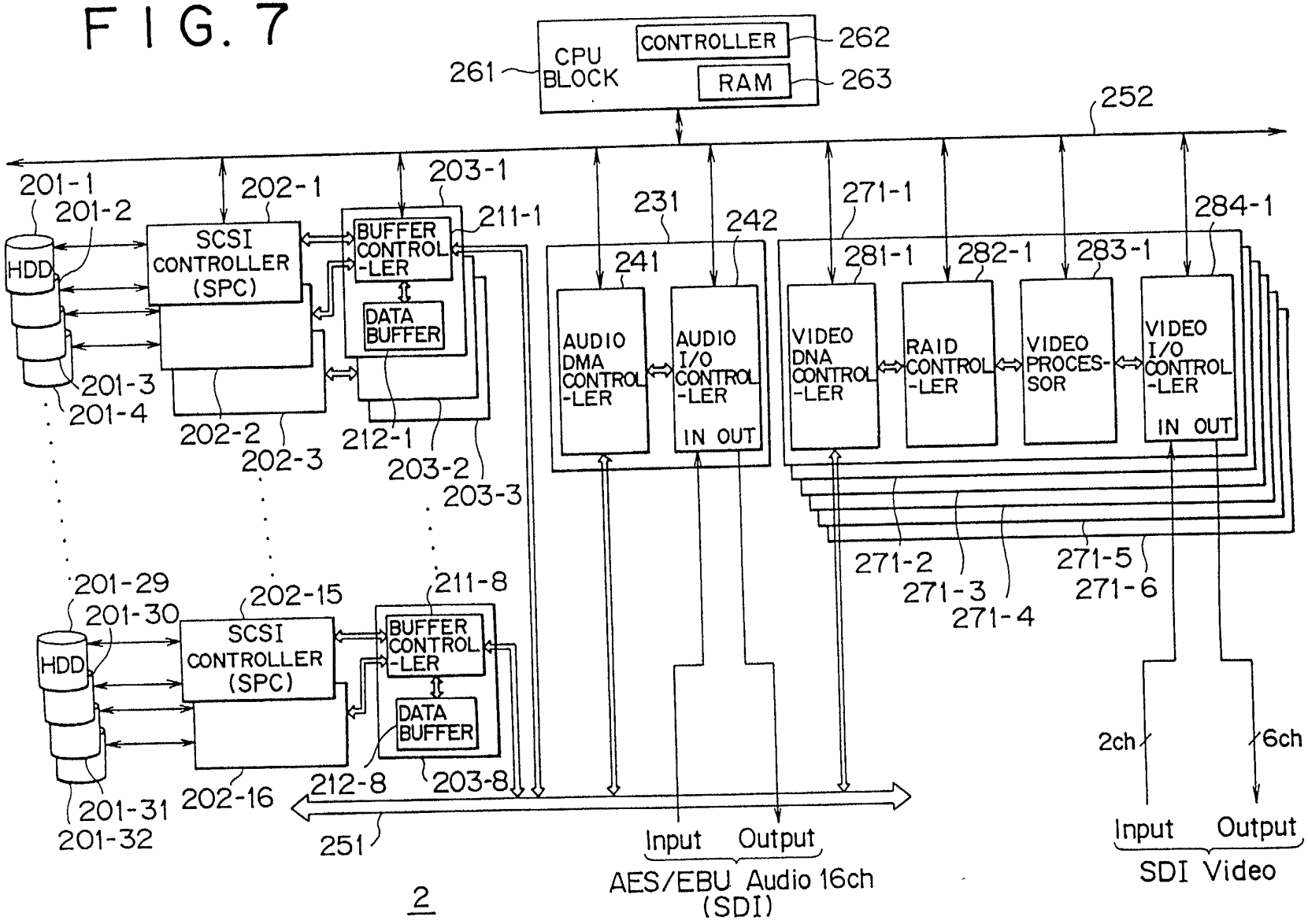

261
CPU BLOCK
CONTROLLER
262
RAM
263
252
201-1
201-2
HDD
SCSI CONTROLLER (SPC)
202-1
BUFFER CONTROL -LER
DATA BUFFER
203-1
211-1
231
241
242
AUDIO DMA CONTROL -LER
AUDIO I/O CONTROL -LER
IN OUT
271-1
281-1
282-1
283-1
284-1
VIDEO DNA CONTROL -LER
RAID CONTROL -LER
VIDEO PROCES- SOR
VIDEO I/O CONTROL -LER
IN OUT
201-3
201-4
202-2
202-3
212-1
203-2
203-3
271-2
271-3
271-4
271-5
271-6
201-29
201-30
HDD
SCSI CONTROLLER (SPC)
202-15
BUFFER CONTROL -LER
DATA BUFFER
211-8
212-8
203-8
201-31
201-32
202-16
251
2ch
6ch
Input
Output
AES/EBU Audio 16ch (SDI)
Input
Output
SDI Video
2

FIG.8

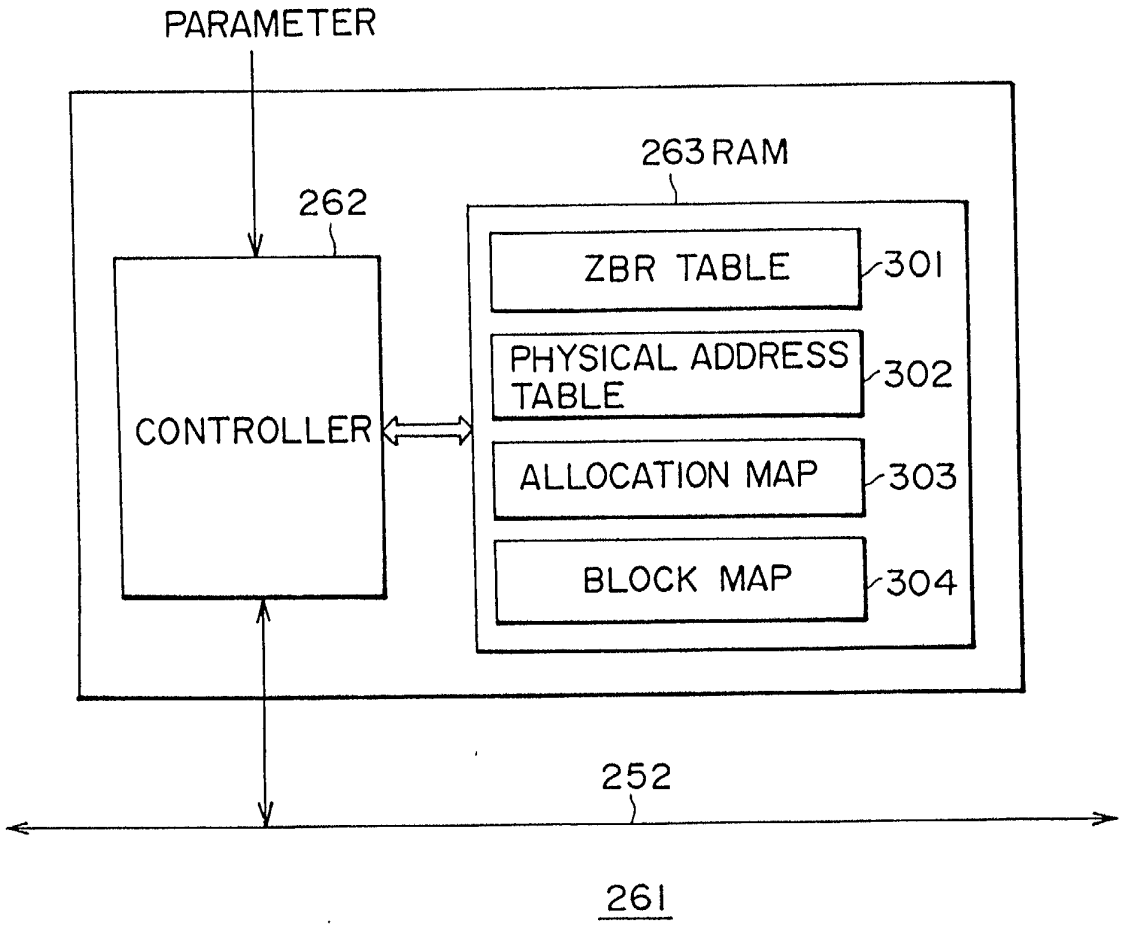

PARAMETER
263 RAM
262
ZBR TABLE
301
PHYSICAL ADDRESS TABLE
302
CONTROLLER
ALLOCATION MAP
303
BLOCK MAP
304
252
261

FIG. 9

ZBR TABLE (NTSC)

ZONE	CYLINDER ADDRESS	NUMBER OF SECTORS	
1	0001-0500	567	(OUTER CIRCUMFERENCE)
2	0501-1000	544	
3	1001-1500	536	
4	1501-2000	518	
5	2001-2500	498	
6	2501-3000	480	
7	3001-3500	480	
8	3501-4000	462	
9	4001-4500	442	
10	4501-5000	424	
11	5001-5500	416	
12	5501-6000	393	(INNER CIRCUMFERENCE)

FIG. 10

ZBR TABLE (PAL)

ZONE	CYLINDER ADDRESS	NUMBER OF SECTORS	
1	0001-0500	561	(OUTER CIRCUMFERENCE)
2	0501-1000	534	
3	1001-1500	525	
4	1501-2000	501	
5	2001-2500	480	
6	2501-3000	459	
7	3001-3500	459	
8	3501-4000	445	
9	4001-4500	431	
10	4501-5000	415	
11	5001-5500	409	
12	5501-6000	391	(INNER CIRCUMFERENCE)

FIG. 11A

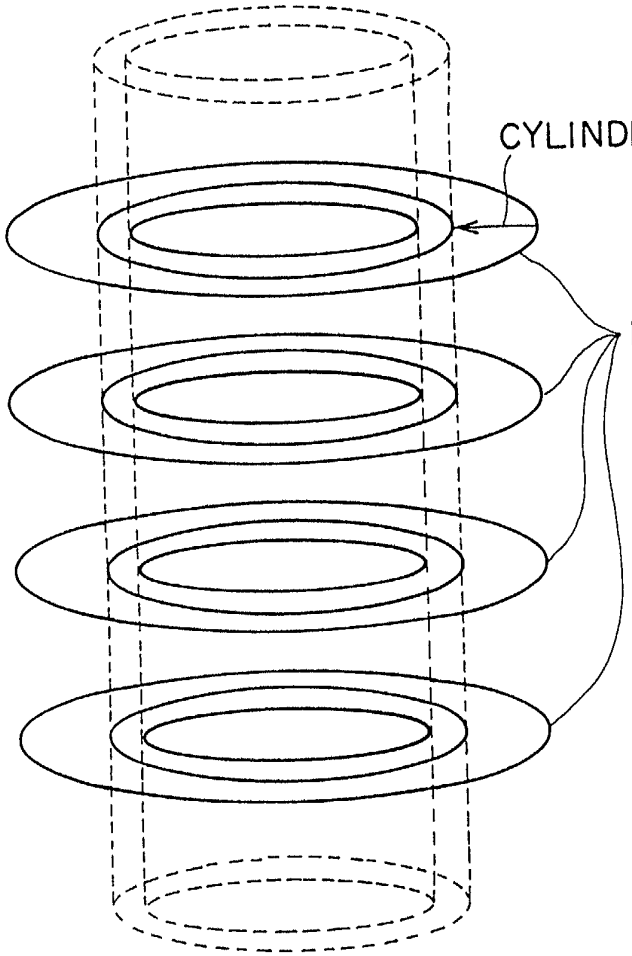


FIG. 11B

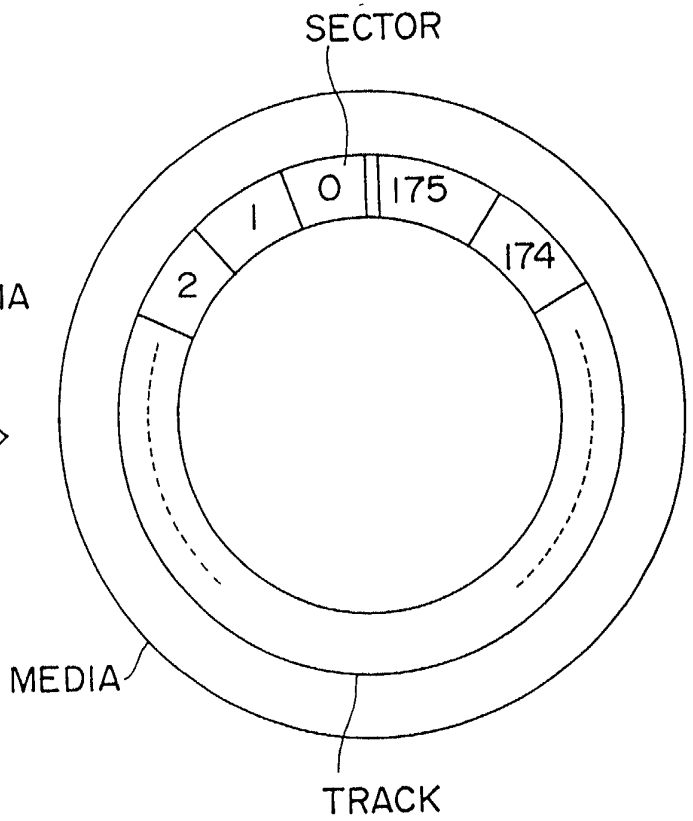


FIG. 12

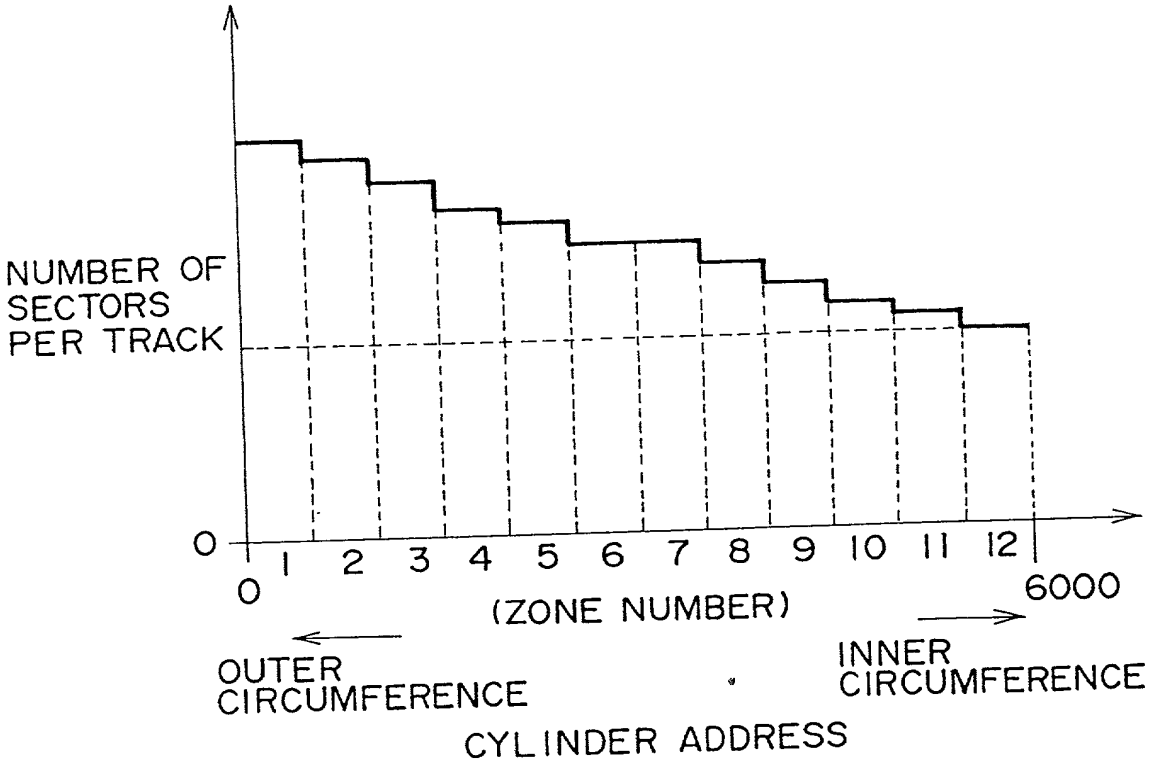

NUMBER OF SECTORS PER TRACK
0
0 1 2 3 4 5 6 7 8 9 10 11 12
(ZONE NUMBER)
6000
OUTER CIRCUMFERENCE
INNER CIRCUMFERENCE
CYLINDER ADDRESS

FIG. 13A

LOGICAL SECTOR	CYLINDER	MEDIA	SECTOR
Lki	CYLki	MEDki	SECki

FIG. 14

DATA NO.		DISK ID	LOGICAL SECTOR	SIZE
k	p	Dkp	Lkp	Skp
		Dk1	Lk1	Sk1
		Dk2	Lk2	Sk2
		:	:	:
		Dkn	Lkn	Skn

304

FIG. 13B

LOGICAL SECTOR	CYLINDER	MEDIA	SECTOR
0	0	0	0
1	0	0	1
2	0	0	2
3	0	0	3
4	0	0	4
5	0	0	5
6	0	0	6
7	0	0	7
⋮	⋮	⋮	⋮

302

FIG. 15

FRAME NO.	DISK ID	START LOGICAL SECTOR	SECTOR SIZE	
1	1	0	567	← PARITY DATA (P1)
	2	599600	393	← FIRST SUBBLOCK DATA (S1-1)
	3	0	567	← SECOND SUBBLOCK DATA (S1-2)
	4	599600	393	← THIRD SUBBLOCK DATA (S1-3)
	5	0	567	← FOURTH SUBBLOCK DATA (S1-4)
2	2	0	567	← PARITY DATA (P2)
	3	599600	393	← FIRST SUBBLOCK DATA (S2-1)
	4	0	567	← SECOND SUBBLOCK DATA (S2-2)
	5	599600	393	← THIRD SUBBLOCK DATA (S2-3)
	6	0	567	← FOURTH SUBBLOCK DATA (S2-4)
3	3	600	567	← PARITY DATA (P3)
	4	599200	393	← FIRST SUBBLOCK DATA (S3-1)
	5	600	567	← SECOND SUBBLOCK DATA (S3-2)
	6	599600	393	← THIRD SUBBLOCK DATA (S3-3)
	1	600	567	← FOURTH SUBBLOCK DATA (S3-4)
4	4	600	567	← PARITY DATA (P4)
	5	599200	393	← FIRST SUBBLOCK DATA (S4-1)
	6	600	567	← SECOND SUBBLOCK (S4-2)
	1	599600	393	← THIRD SUBBLOCK DATA (S4-3)
	2	600	567	← FOURTH SUBBLOCK DATA (S4-4)
⋮	⋮	⋮	⋮	

304

FIG. 16

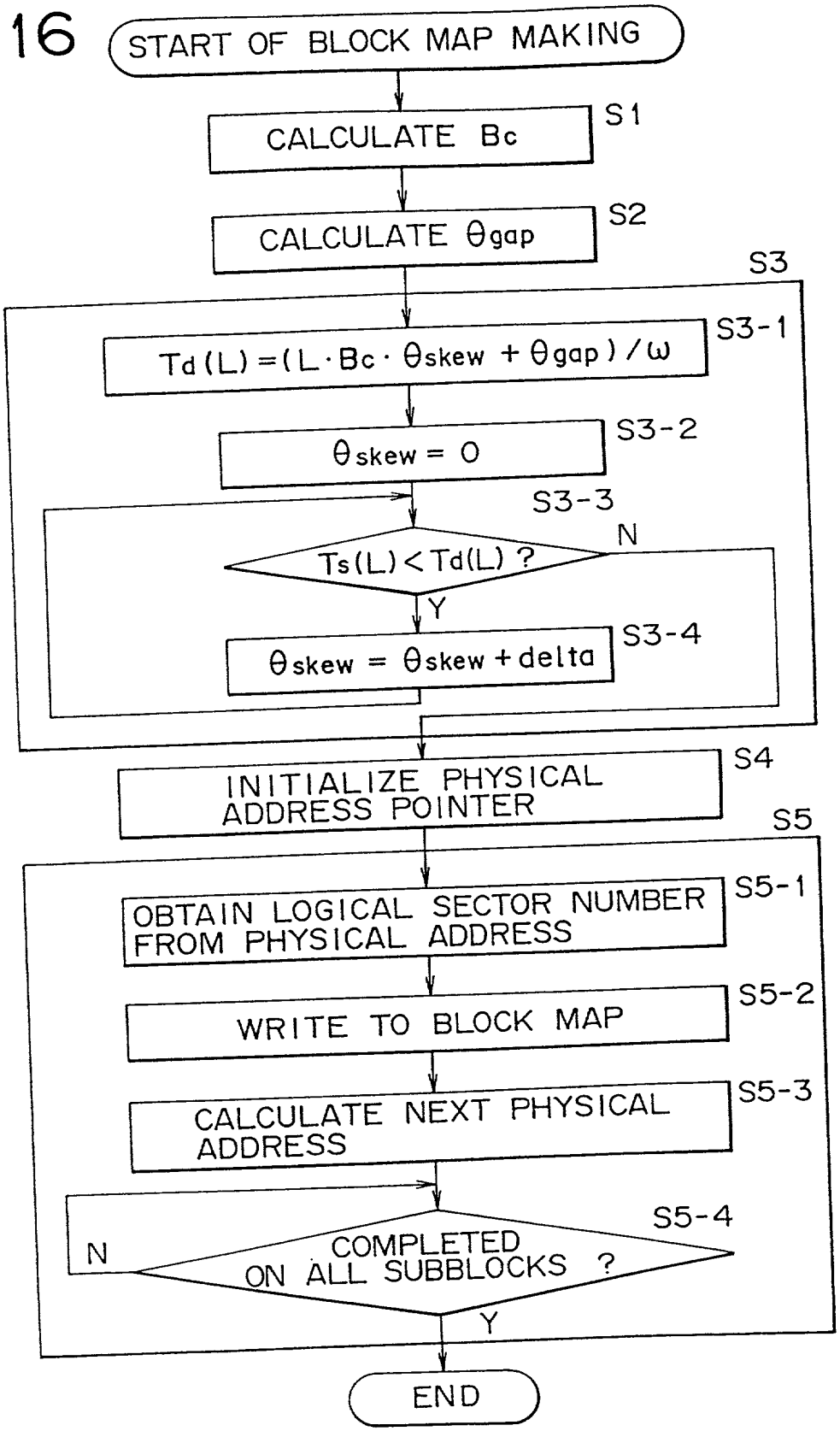

START OF BLOCK MAP MAKING
CALCULATE Bc
S1
CALCULATE θgap
S2
S3
Td(L)=(L·Bc·θskew + θgap)/ω
S3-1
θskew = 0
S3-2
S3-3
Ts(L) < Td(L) ?
N
Y
θskew = θskew + delta
S3-4
INITIALIZE PHYSICAL ADDRESS POINTER
S4
S5
OBTAIN LOGICAL SECTOR NUMBER FROM PHYSICAL ADDRESS
S5-1
WRITE TO BLOCK MAP
S5-2
CALCULATE NEXT PHYSICAL ADDRESS
S5-3
S5-4
N
COMPLETED ON ALL SUBBLOCKS ?
Y
END

FIG. 17

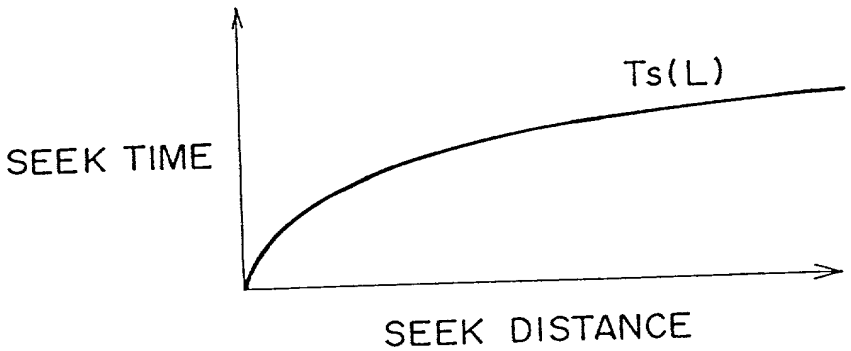

Ts(L)
SEEK TIME
SEEK DISTANCE

FIG. 18

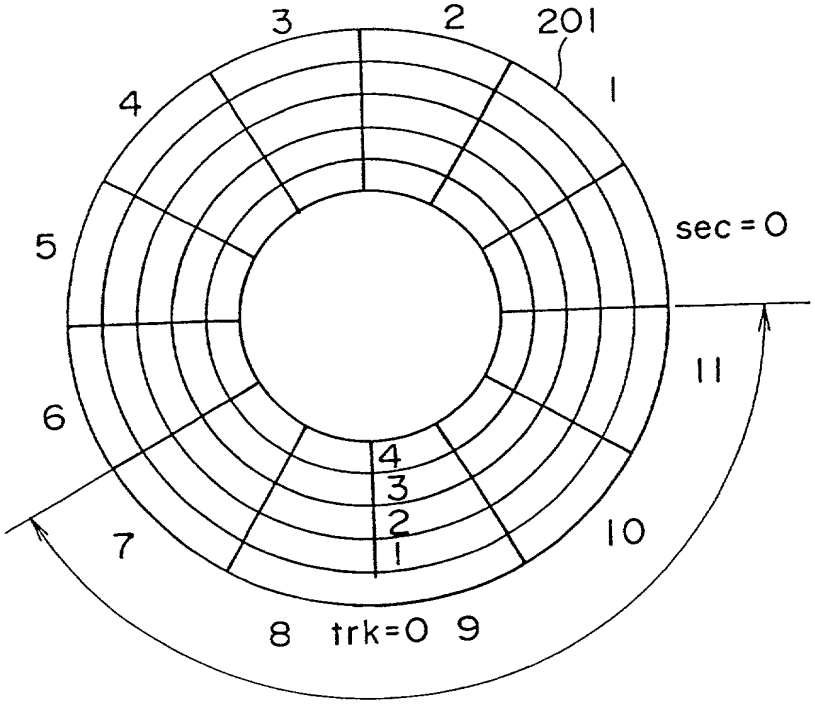

3
2
201
1
4
5
sec=0
11
6
4
3
2
1
7
10
8
trk=0
9

FIG. 19

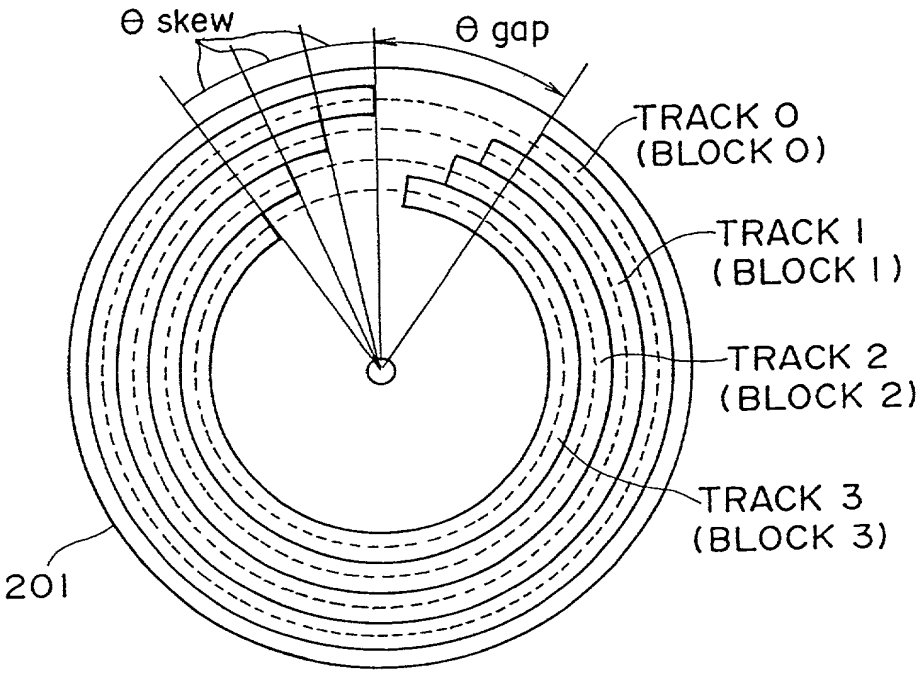

θ skew
θ gap
TRACK 0
(BLOCK 0)
TRACK 1
(BLOCK 1)
TRACK 2
(BLOCK 2)
TRACK 3
(BLOCK 3)
201

FIG. 20

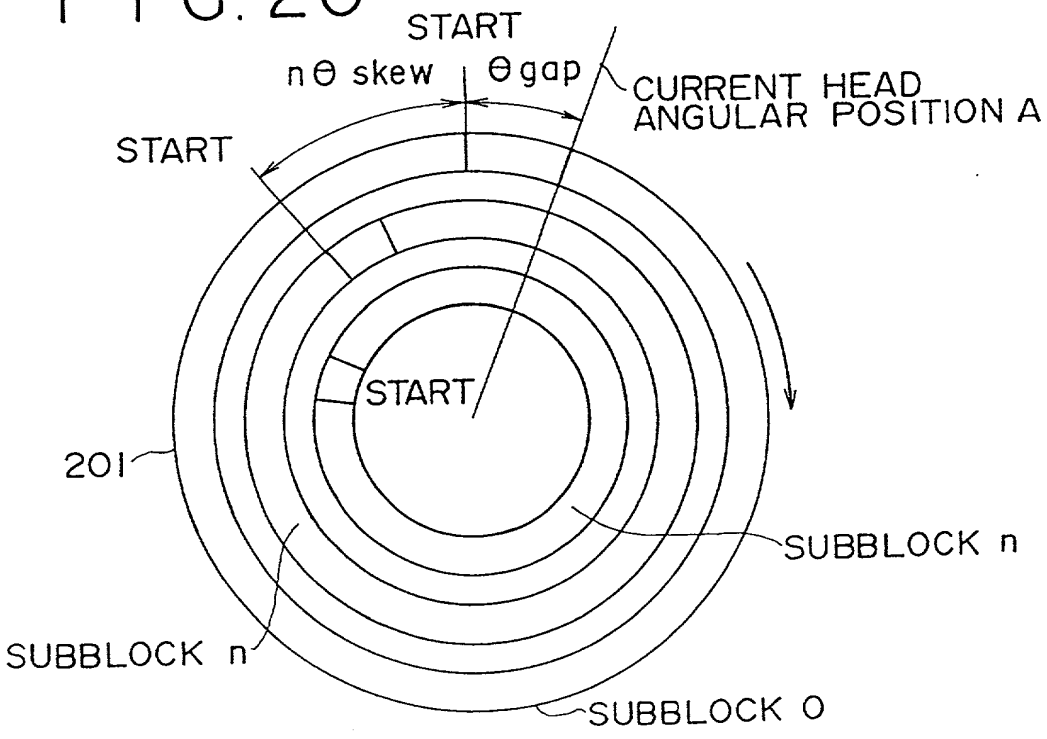

START
nθ skew
θ gap
CURRENT HEAD
ANGULAR POSITION A
START
START
201
SUBBLOCK n
SUBBLOCK n
SUBBLOCK 0

FIG. 21

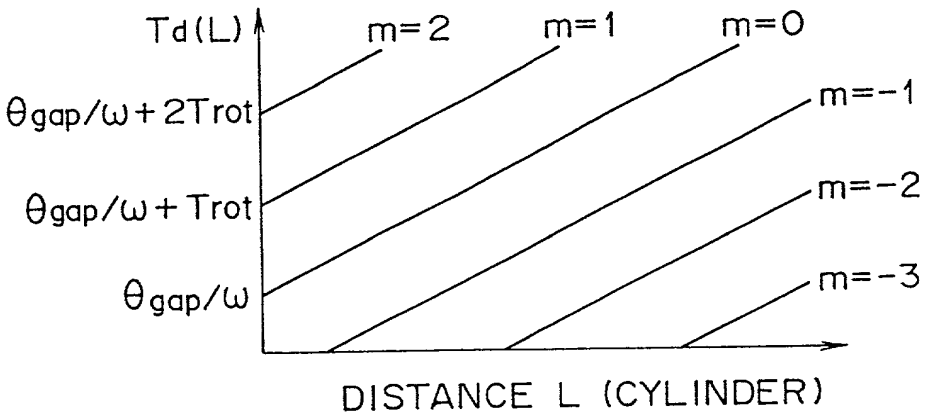

Td(L)
m=2
m=1
m=0
m=-1
m=-2
m=-3
θgap/ω+2Trot
θgap/ω+Trot
θgap/ω
DISTANCE L (CYLINDER)

FIG. 22

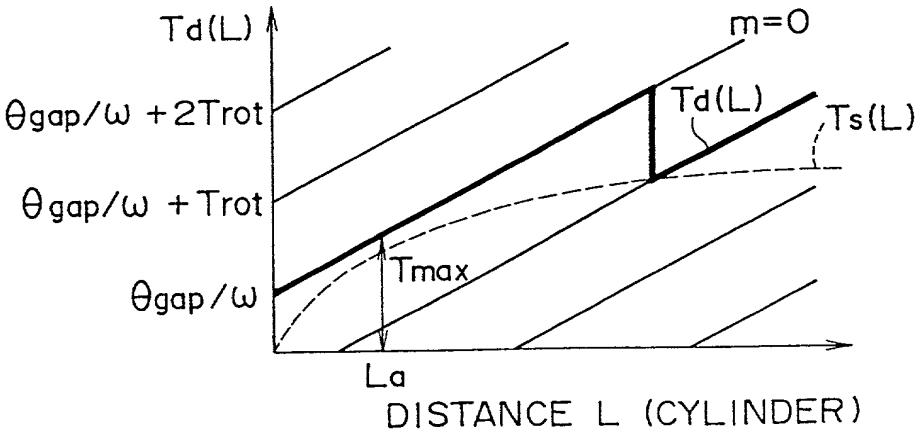

Td(L)
m=0
Td(L)
Ts(L)
θgap/ω +2Trot
θgap/ω +Trot
θgap/ω
Tmax
La
DISTANCE L (CYLINDER)

FIG. 23

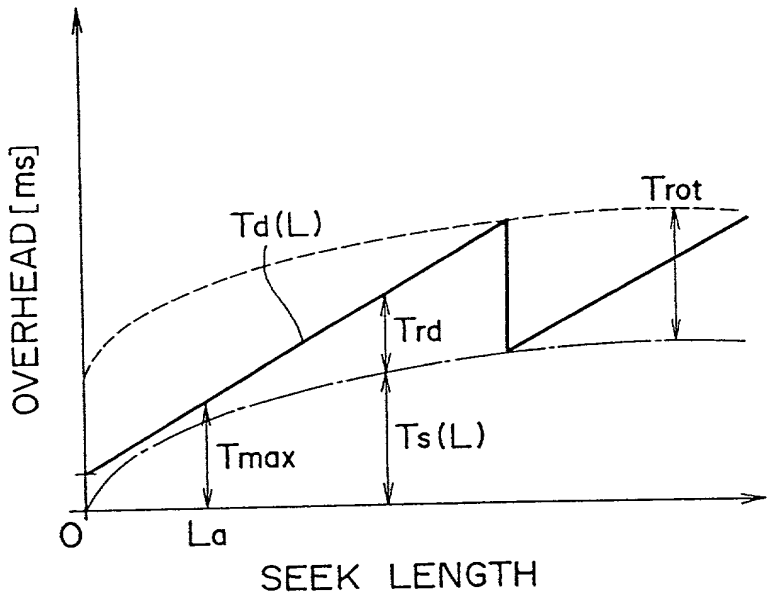


FIG. 24

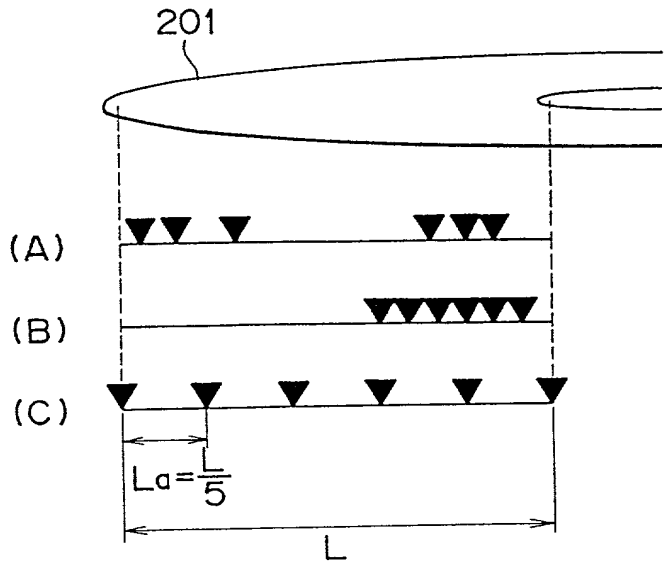

201
(A)
(B)
(C)
La=L/5
L

FIG. 25

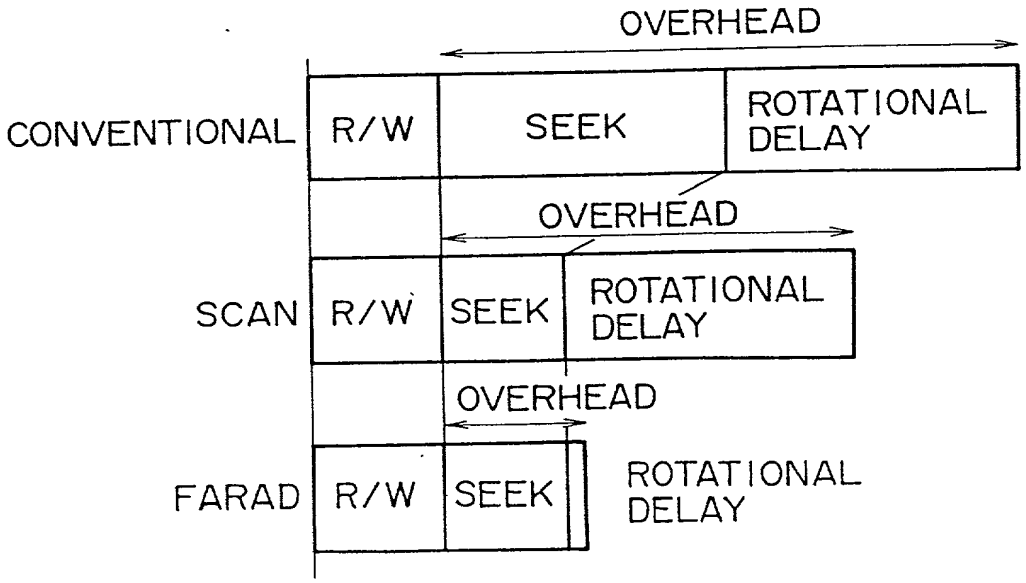

OVERHEAD
CONVENTIONAL
R/W
SEEK
ROTATIONAL DELAY
OVERHEAD
SCAN
R/W
SEEK
ROTATIONAL DELAY
OVERHEAD
FARAD
R/W
SEEK
ROTATIONAL DELAY

FIG. 26

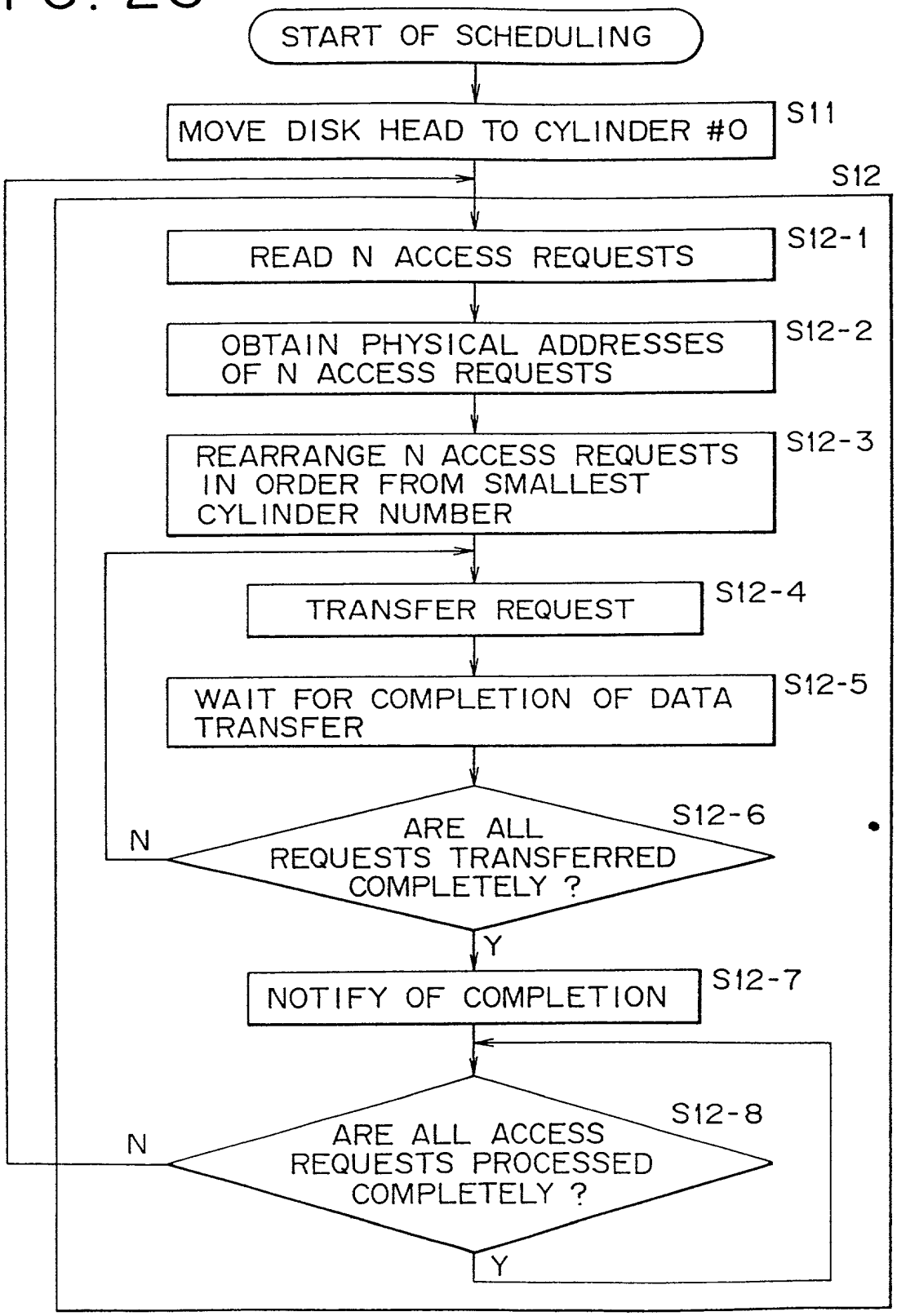

START OF SCHEDULING
MOVE DISK HEAD TO CYLINDER #0
S11
S12
READ N ACCESS REQUESTS
S12-1
OBTAIN PHYSICAL ADDRESSES OF N ACCESS REQUESTS
S12-2
REARRANGE N ACCESS REQUESTS IN ORDER FROM SMALLEST CYLINDER NUMBER
S12-3
TRANSFER REQUEST
S12-4
WAIT FOR COMPLETION OF DATA TRANSFER
S12-5
ARE ALL REQUESTS TRANSFERRED COMPLETELY ?
S12-6
N
Y
NOTIFY OF COMPLETION
S12-7
ARE ALL ACCESS REQUESTS PROCESSED COMPLETELY ?
S12-8
N
Y

FIG. 27

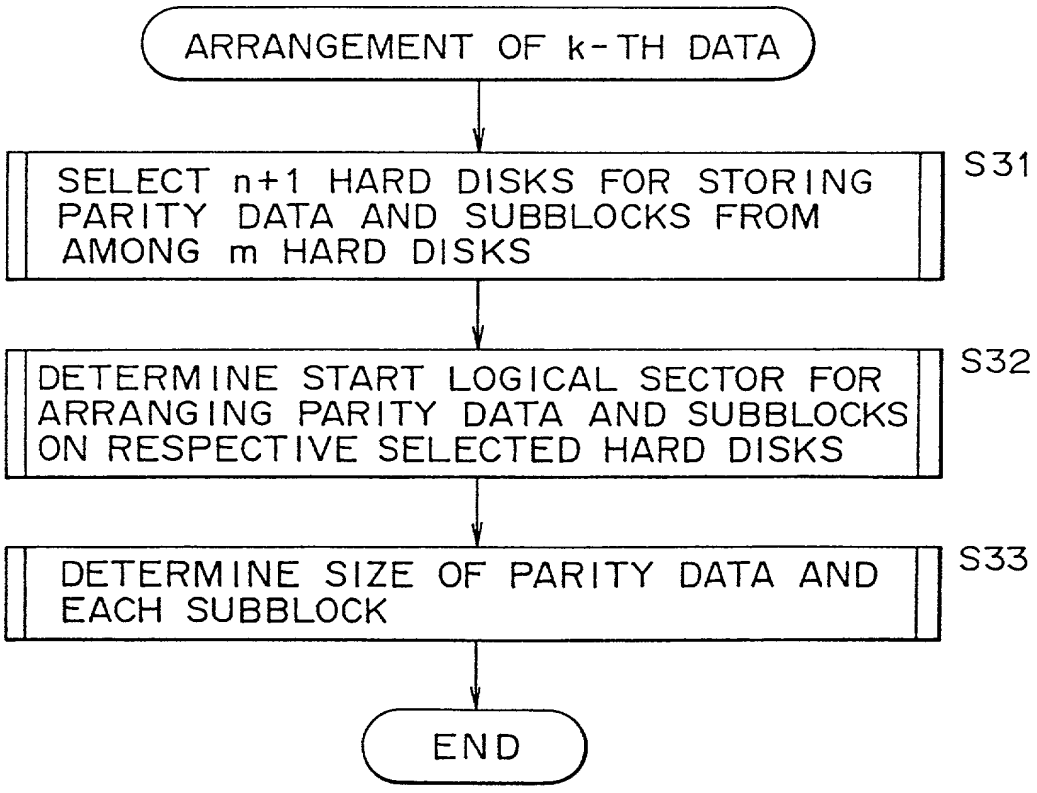

ARRANGEMENT OF k-TH DATA
SELECT n+1 HARD DISKS FOR STORING PARITY DATA AND SUBBLOCKS FROM AMONG m HARD DISKS
S31
DETERMINE START LOGICAL SECTOR FOR ARRANGING PARITY DATA AND SUBBLOCKS ON RESPECTIVE SELECTED HARD DISKS
S32
DETERMINE SIZE OF PARITY DATA AND EACH SUBBLOCK
S33
END

FIG. 28

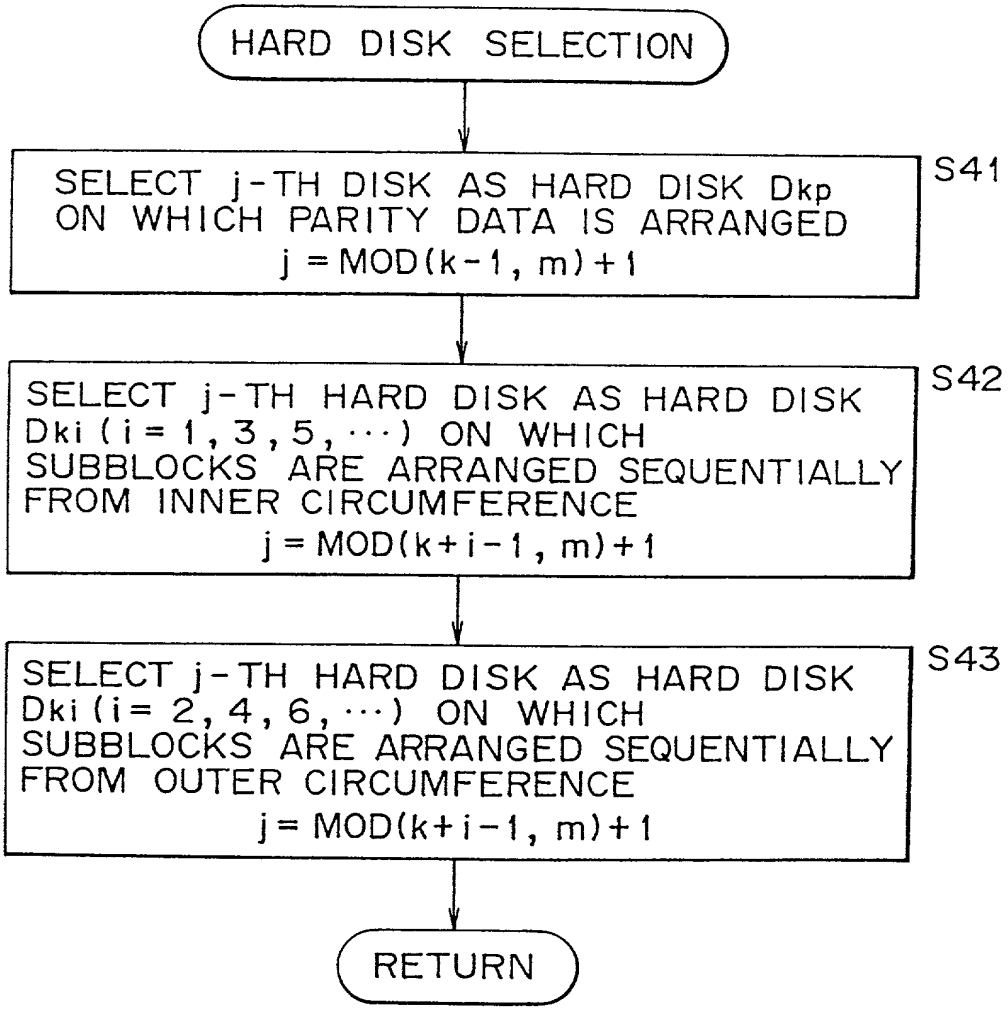

HARD DISK SELECTION
SELECT j-TH DISK AS HARD DISK Dkp ON WHICH PARITY DATA IS ARRANGED
j = MOD(k-1, m)+1
S41
SELECT j-TH HARD DISK AS HARD DISK Dki (i = 1, 3, 5, ···) ON WHICH SUBBLOCKS ARE ARRANGED SEQUENTIALLY FROM INNER CIRCUMFERENCE
j = MOD(k+i-1, m)+1
S42
SELECT j-TH HARD DISK AS HARD DISK Dki (i = 2, 4, 6, ···) ON WHICH SUBBLOCKS ARE ARRANGED SEQUENTIALLY FROM OUTER CIRCUMFERENCE
j = MOD(k+i-1, m)+1
S43
RETURN

FIG. 29

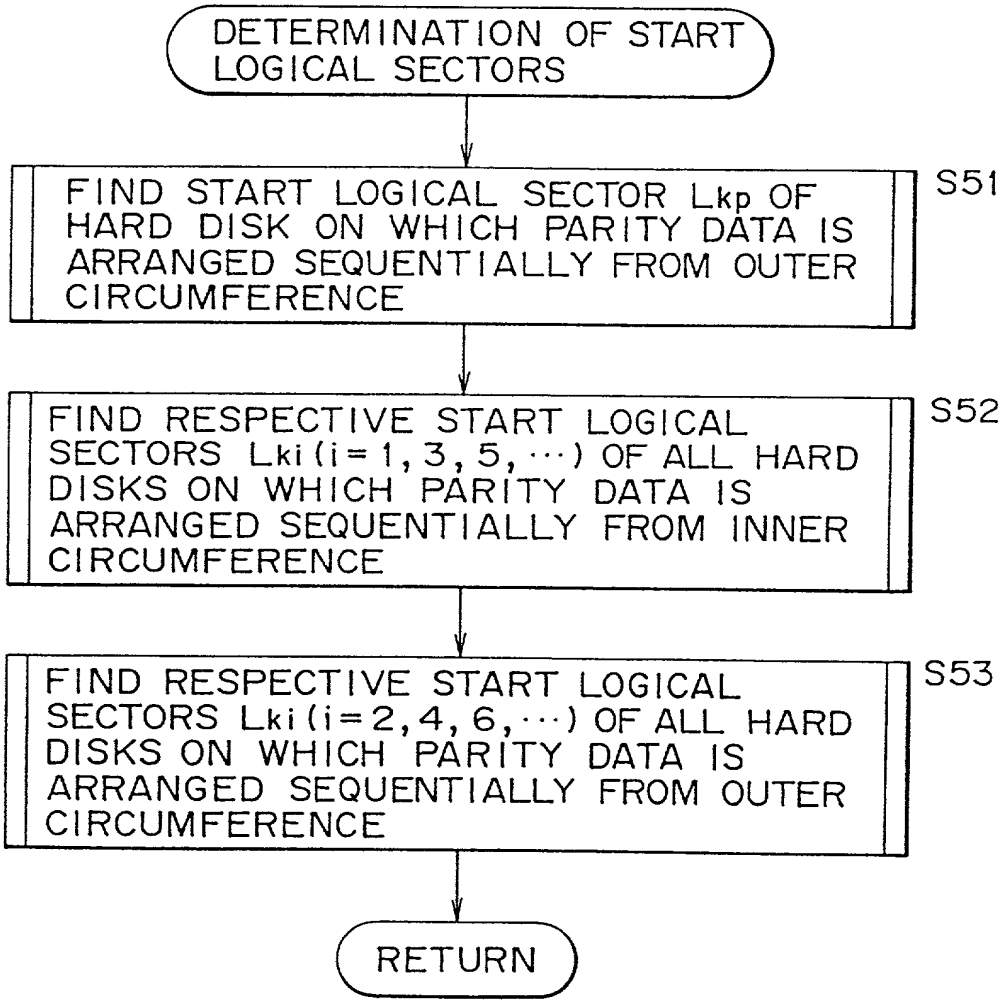

DETERMINATION OF START LOGICAL SECTORS
FIND START LOGICAL SECTOR Lkp OF HARD DISK ON WHICH PARITY DATA IS ARRANGED SEQUENTIALLY FROM OUTER CIRCUMFERENCE
S51
FIND RESPECTIVE START LOGICAL SECTORS Lki (i = 1, 3, 5, ···) OF ALL HARD DISKS ON WHICH PARITY DATA IS ARRANGED SEQUENTIALLY FROM INNER CIRCUMFERENCE
S52
FIND RESPECTIVE START LOGICAL SECTORS Lki (i = 2, 4, 6, ···) OF ALL HARD DISKS ON WHICH PARITY DATA IS ARRANGED SEQUENTIALLY FROM OUTER CIRCUMFERENCE
S53
RETURN

FIG. 30

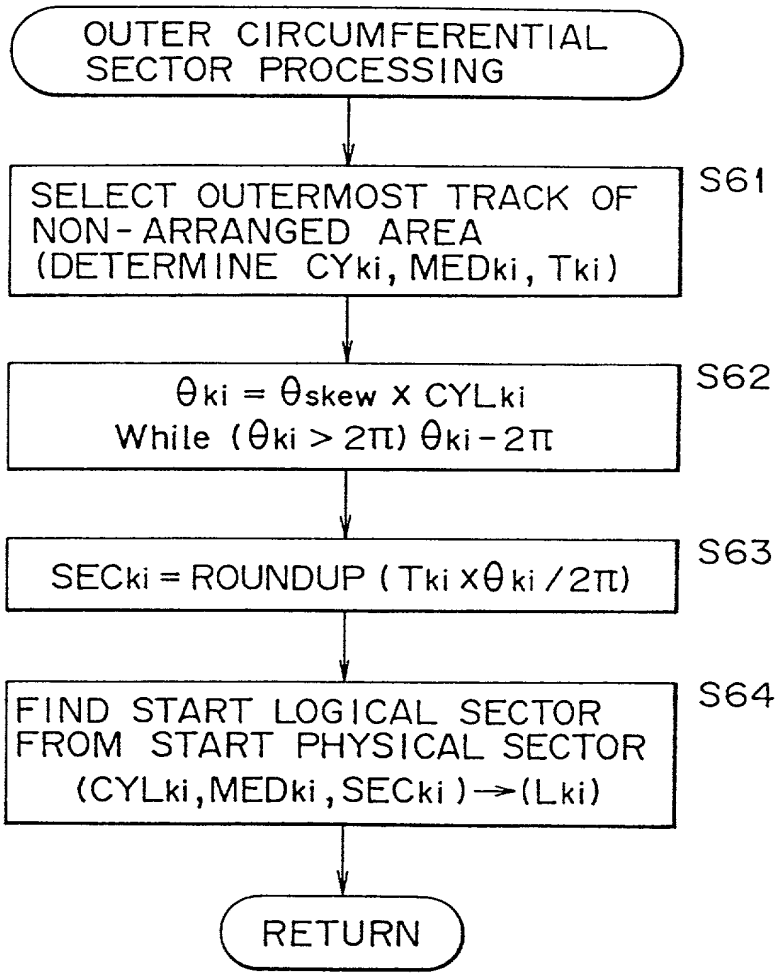

OUTER CIRCUMFERENTIAL SECTOR PROCESSING
SELECT OUTERMOST TRACK OF NON-ARRANGED AREA (DETERMINE CYki, MEDki, Tki)
S61
θki = θskew X CYLki
While (θki > 2π) θki - 2π
S62
SECki = ROUNDUP (Tki x θki / 2π)
S63
FIND START LOGICAL SECTOR FROM START PHYSICAL SECTOR
(CYLki, MEDki, SECki) → (Lki)
S64
RETURN

FIG. 31

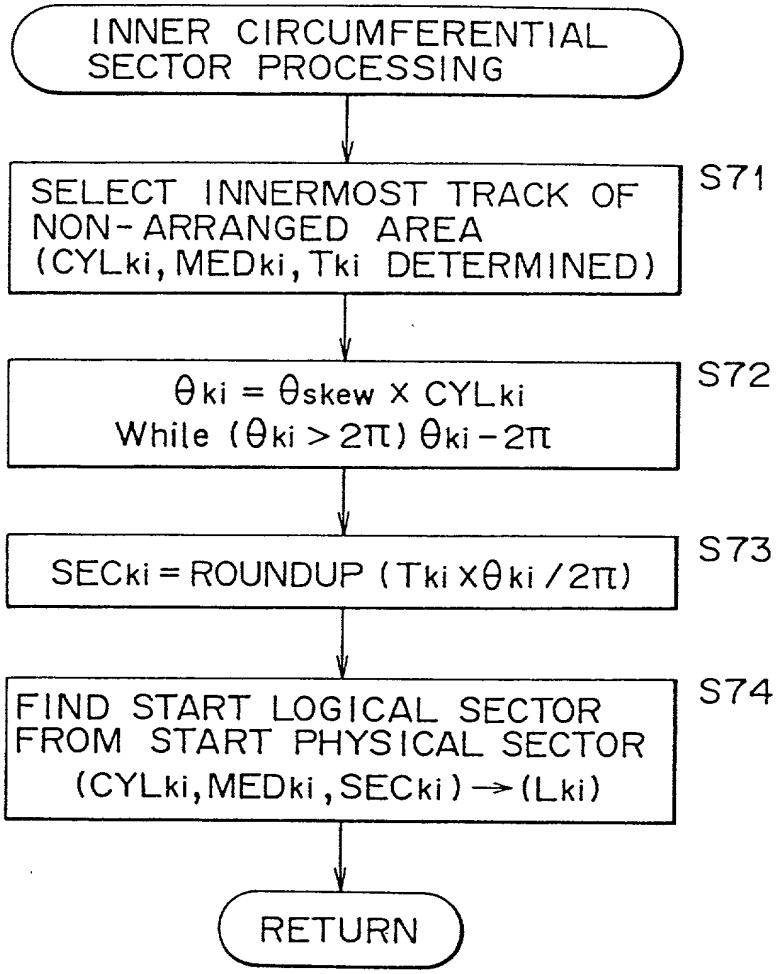

INNER CIRCUMFERENTIAL SECTOR PROCESSING
SELECT INNERMOST TRACK OF NON-ARRANGED AREA (CYLki, MEDki, Tki DETERMINED)
S71
θki = θskew × CYLki
While (θki > 2π) θki − 2π
S72
SECki = ROUNDUP (Tki × θki / 2π)
S73
FIND START LOGICAL SECTOR FROM START PHYSICAL SECTOR
(CYLki, MEDki, SECki) → (Lki)
S74
RETURN

FIG. 32

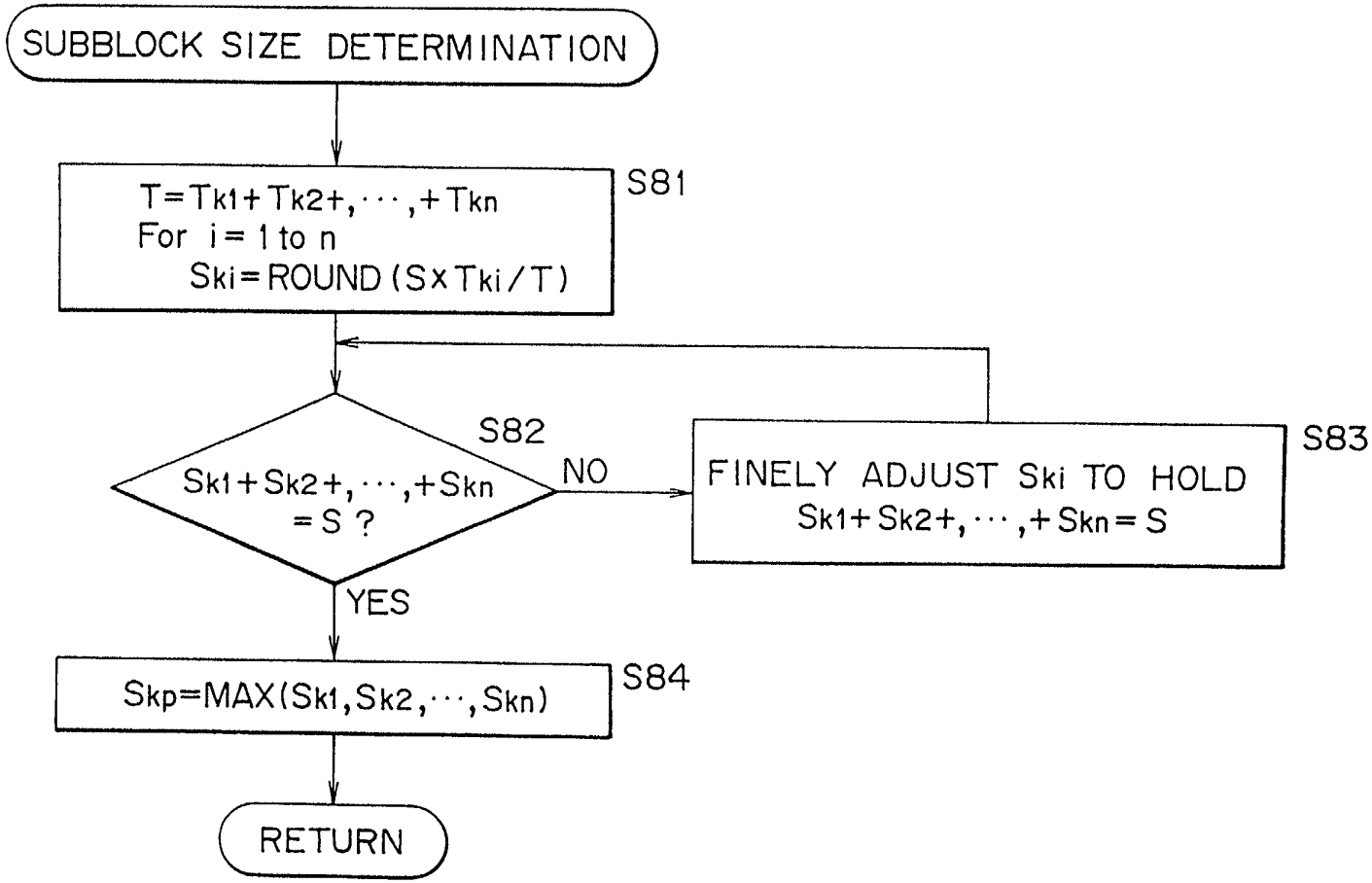

SUBBLOCK SIZE DETERMINATION
T=Tk1+Tk2+,···,+Tkn
For i=1 to n
Ski=ROUND(S×Tki/T)
S81
S82
Sk1+Sk2+,···,+Skn =S ?
NO
FINELY ADJUST Ski TO HOLD Sk1+Sk2+,···,+Skn=S
S83
YES
Skp=MAX(Sk1,Sk2,···,Skn)
S84
RETURN

FIG.33

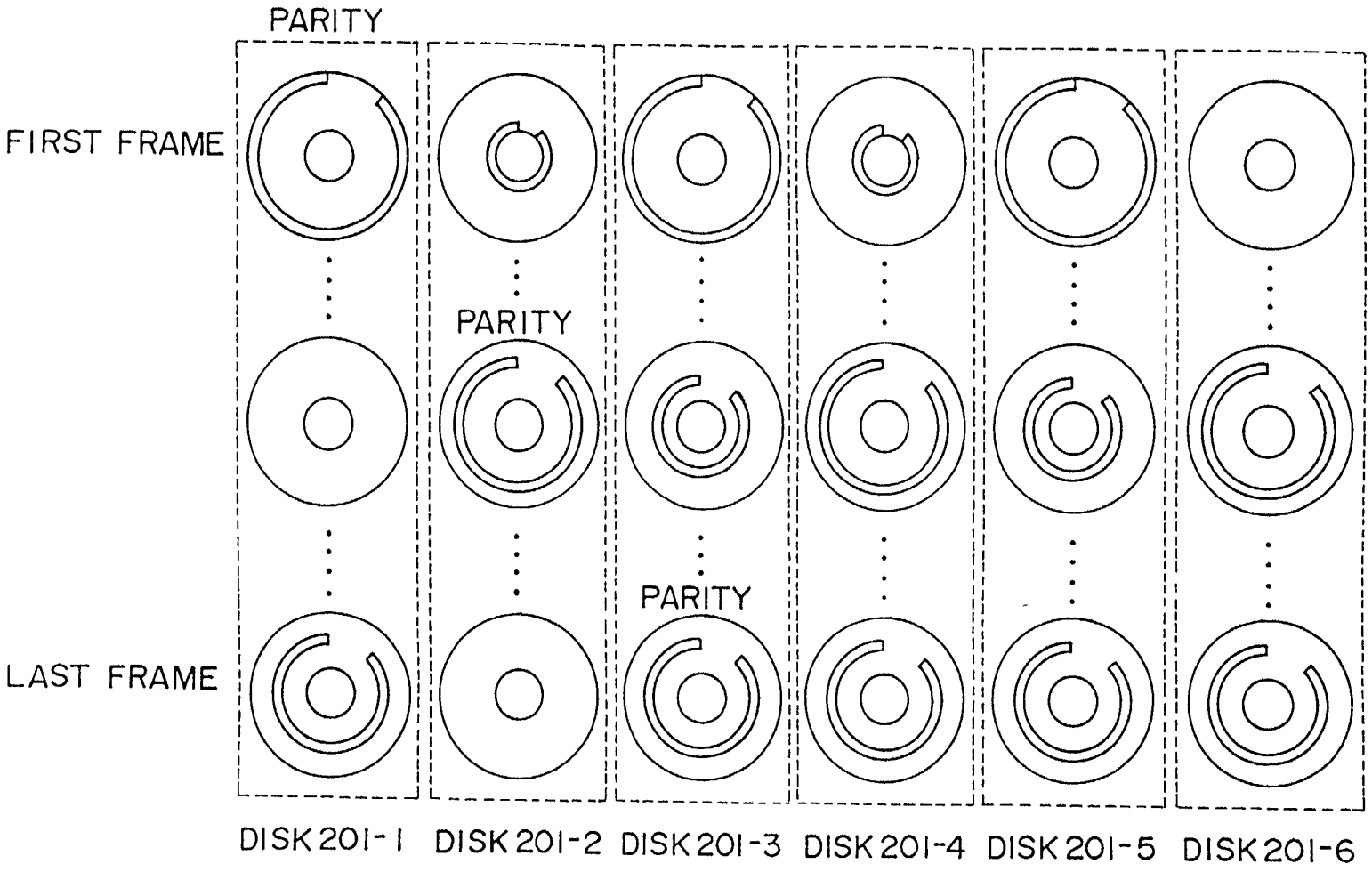


FIG. 34A

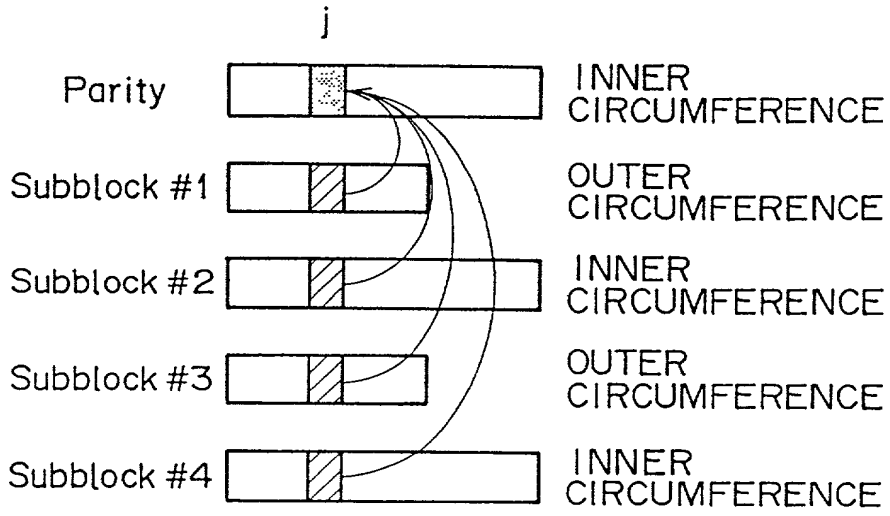


FIG. 34B

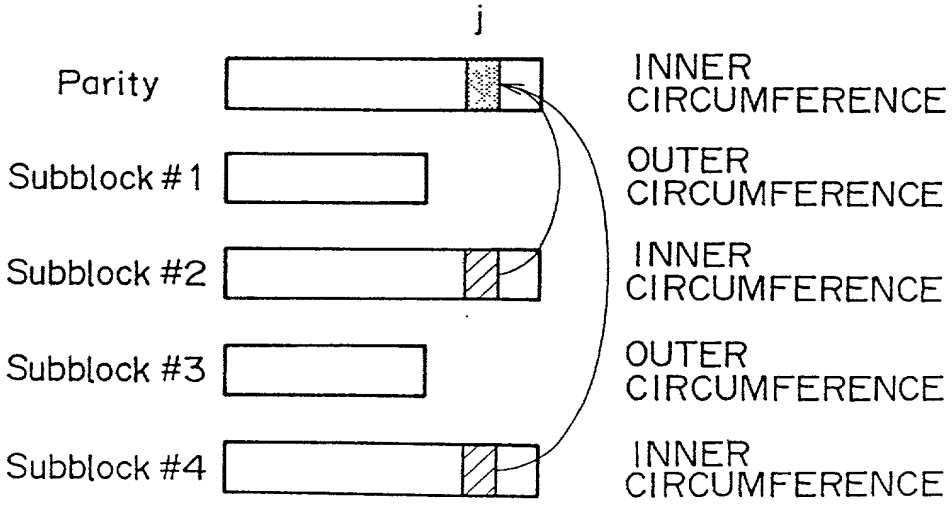


FIG.35A

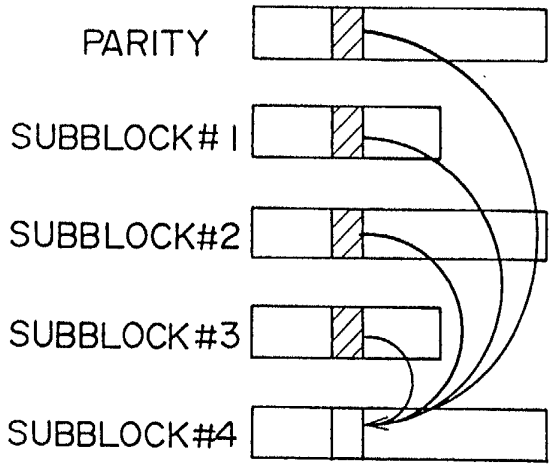


FIG.35B

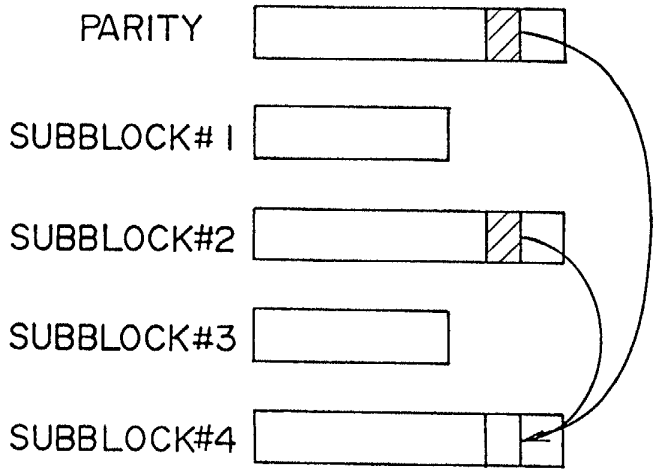


FIG. 36

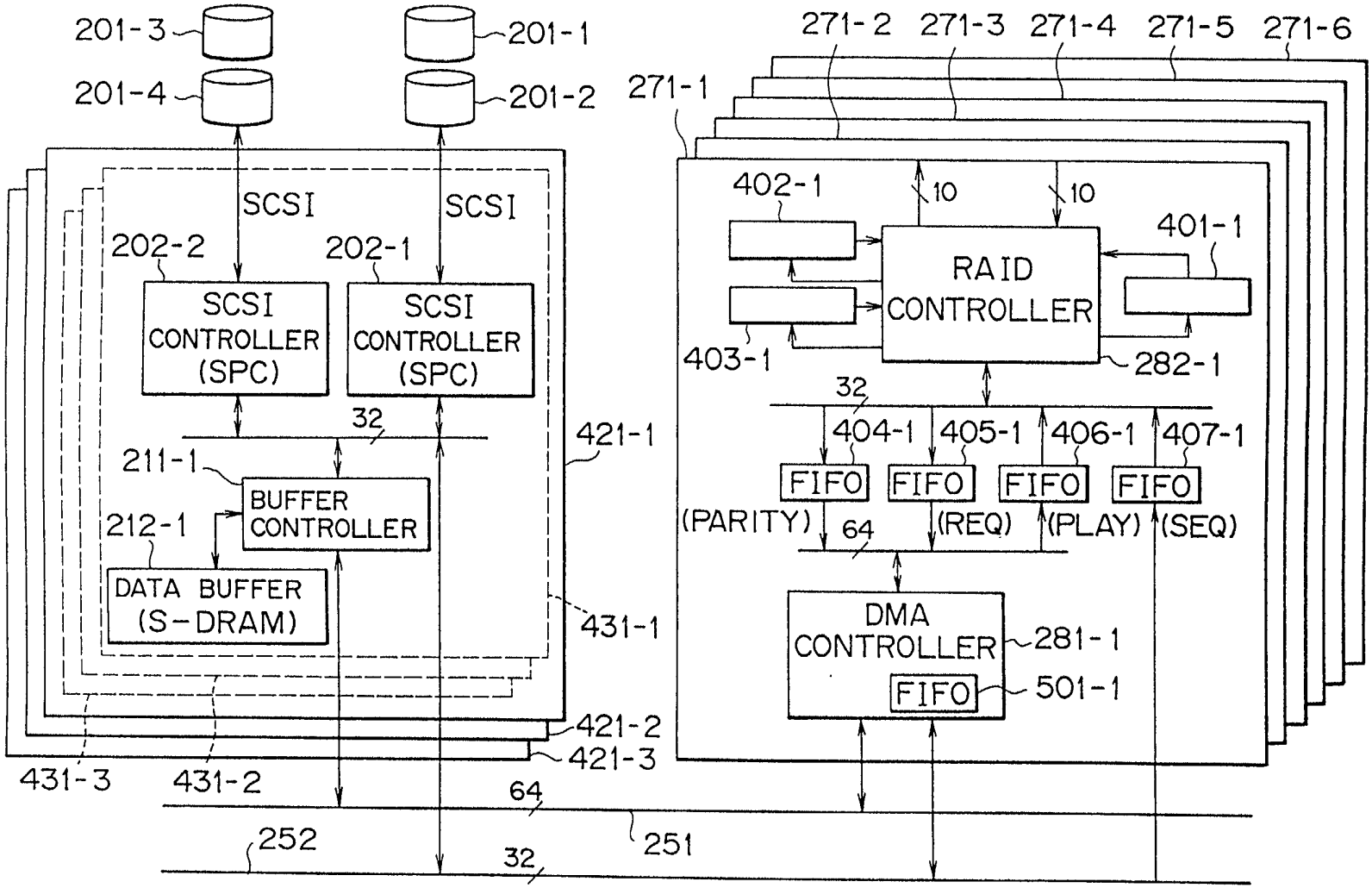

201-3
201-4
201-1
201-2
SCSI
SCSI
202-2
202-1
SCSI CONTROLLER (SPC)
SCSI CONTROLLER (SPC)
32
211-1
BUFFER CONTROLLER
212-1
DATA BUFFER (S-DRAM)
421-1
431-1
421-2
421-3
431-3
431-2
64
252
251
32
271-2
271-3
271-4
271-5
271-6
271-1
402-1
10
10
401-1
RAID CONTROLLER
403-1
282-1
32
404-1
405-1
406-1
407-1
FIFO
FIFO
FIFO
FIFO
(PARITY)
64
(REQ)
(PLAY)
(SEQ)
DMA CONTROLLER
281-1
FIFO
501-1

FIG. 37A

10 BITS ↔ 32 BITS CONVERSION

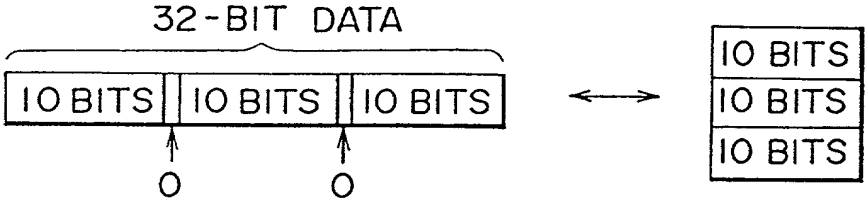


FIG. 37B

8 BITS ↔ 32 BITS CONVERSION

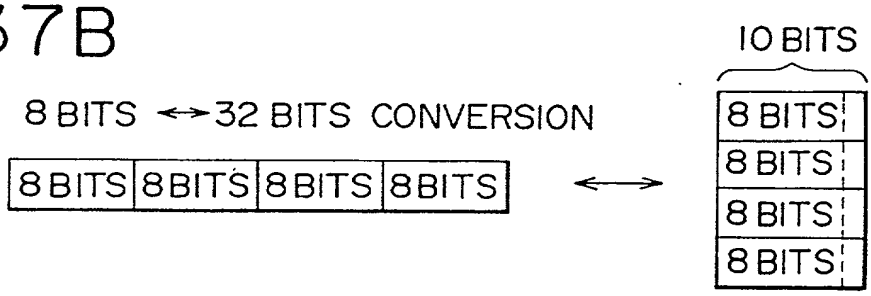


FIG. 38

64 BITS (DMAC) ↔ 32 BITS

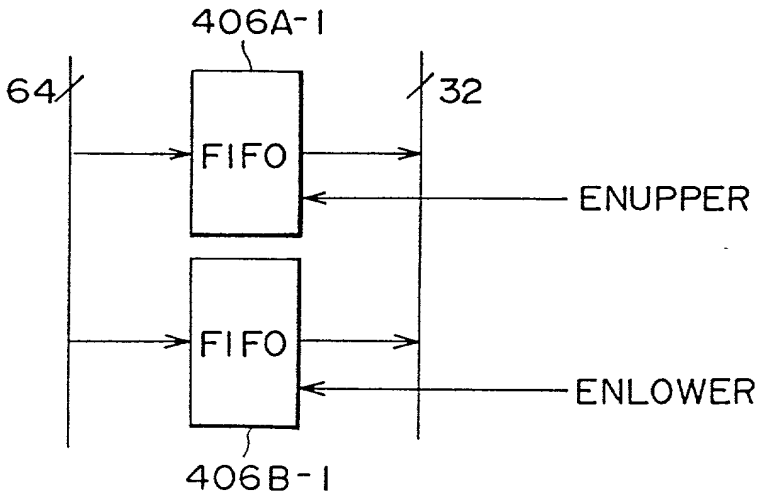


FIG. 39

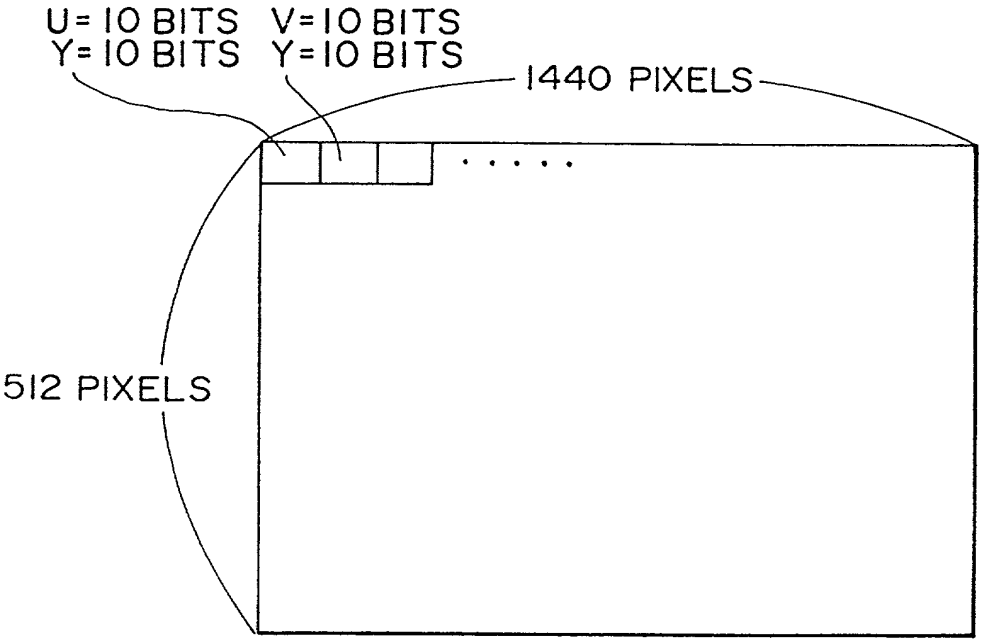

U=10 BITS V=10 BITS
Y=10 BITS Y=10 BITS
1440 PIXELS
512 PIXELS

FIG. 40

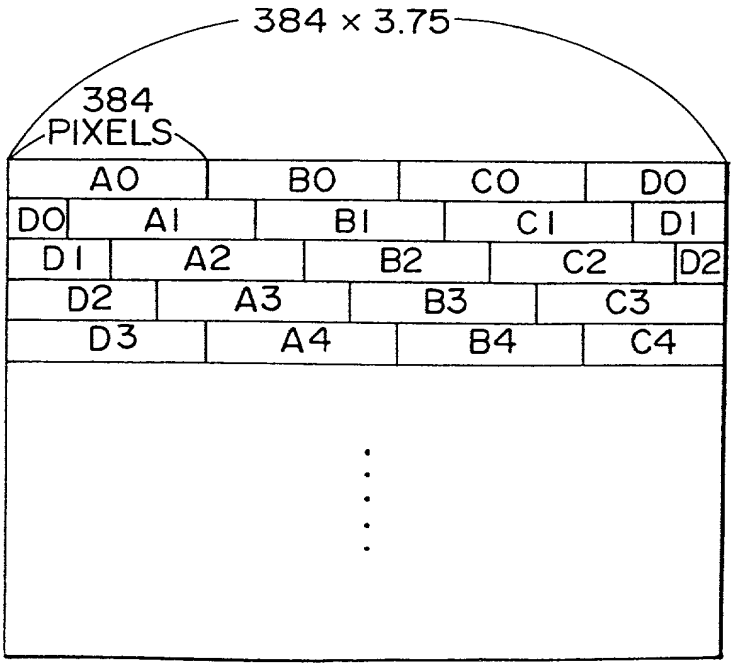

384 x 3.75
384
PIXELS
A0 B0 C0 D0
D0 A1 B1 C1 D1
D1 A2 B2 C2 D2
D2 A3 B3 C3
D3 A4 B4 C4

FIG.41

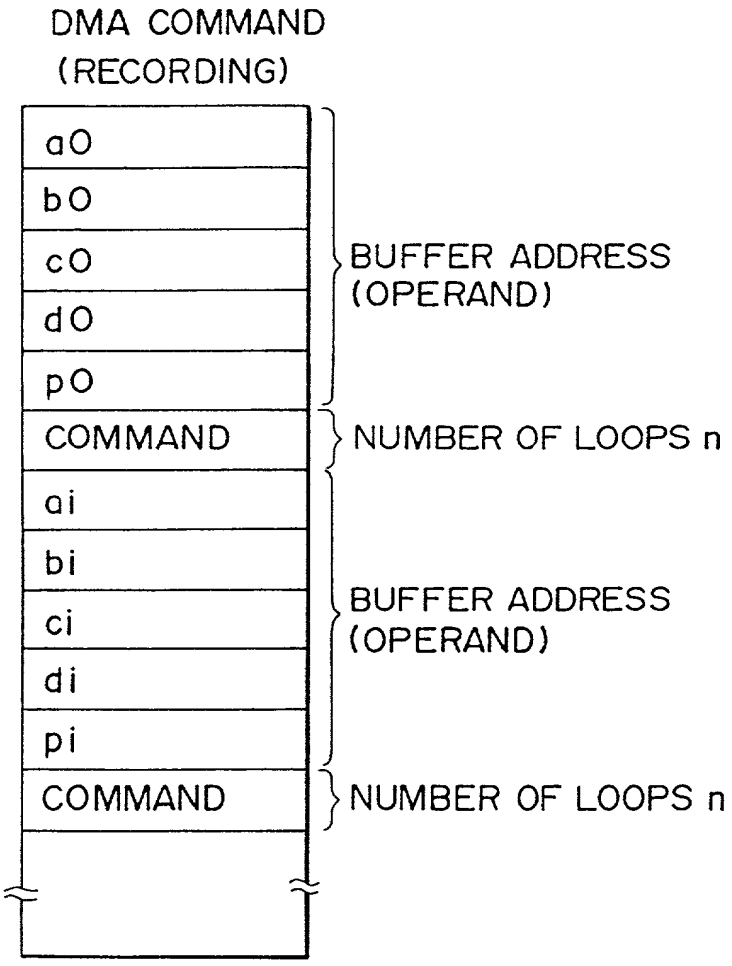

DMA COMMAND
(RECORDING)
aO
bO
cO
dO
pO
COMMAND
ai
bi
ci
di
pi
COMMAND
BUFFER ADDRESS
(OPERAND)
NUMBER OF LOOPS n
BUFFER ADDRESS
(OPERAND)
NUMBER OF LOOPS n

FIG. 42

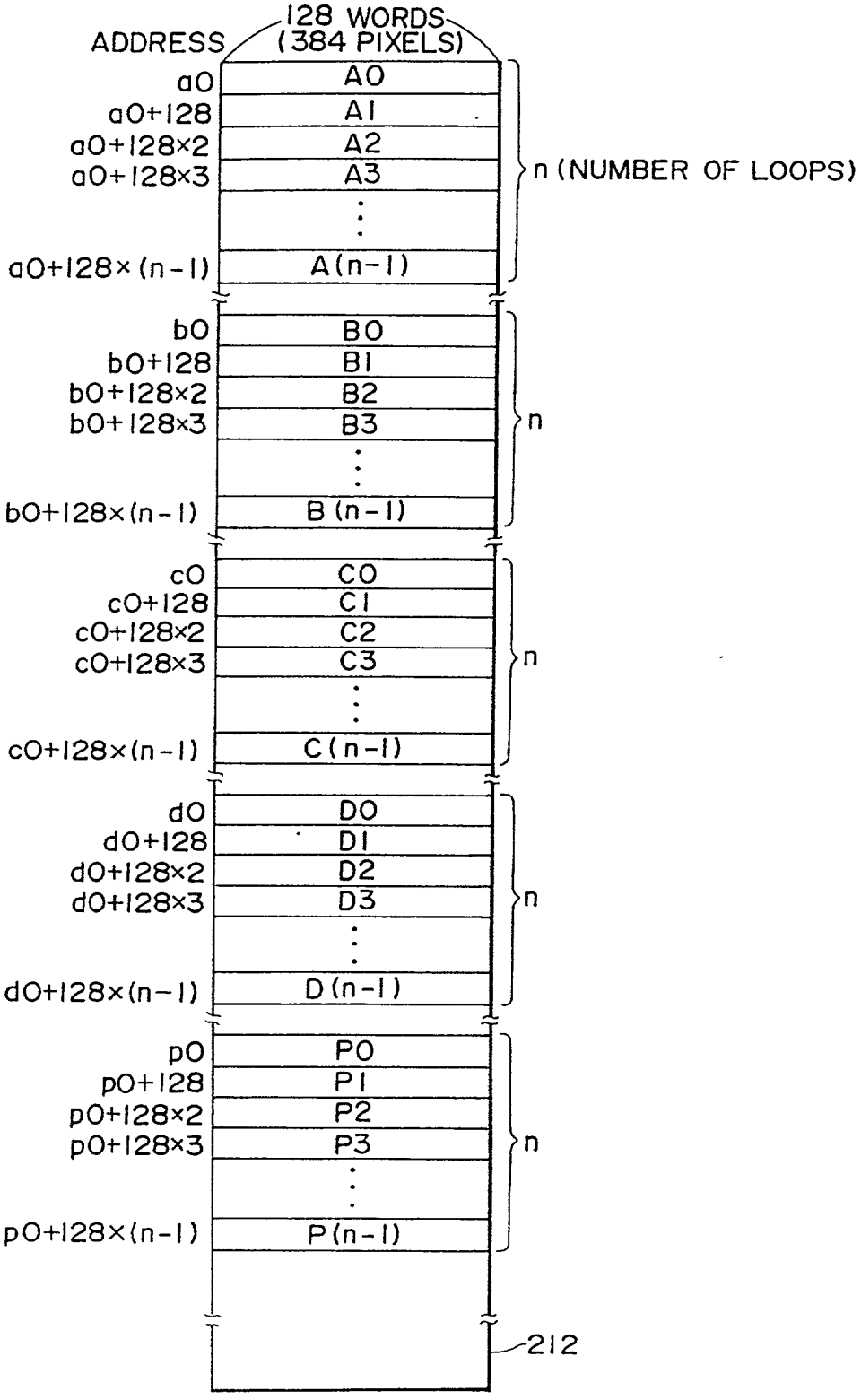
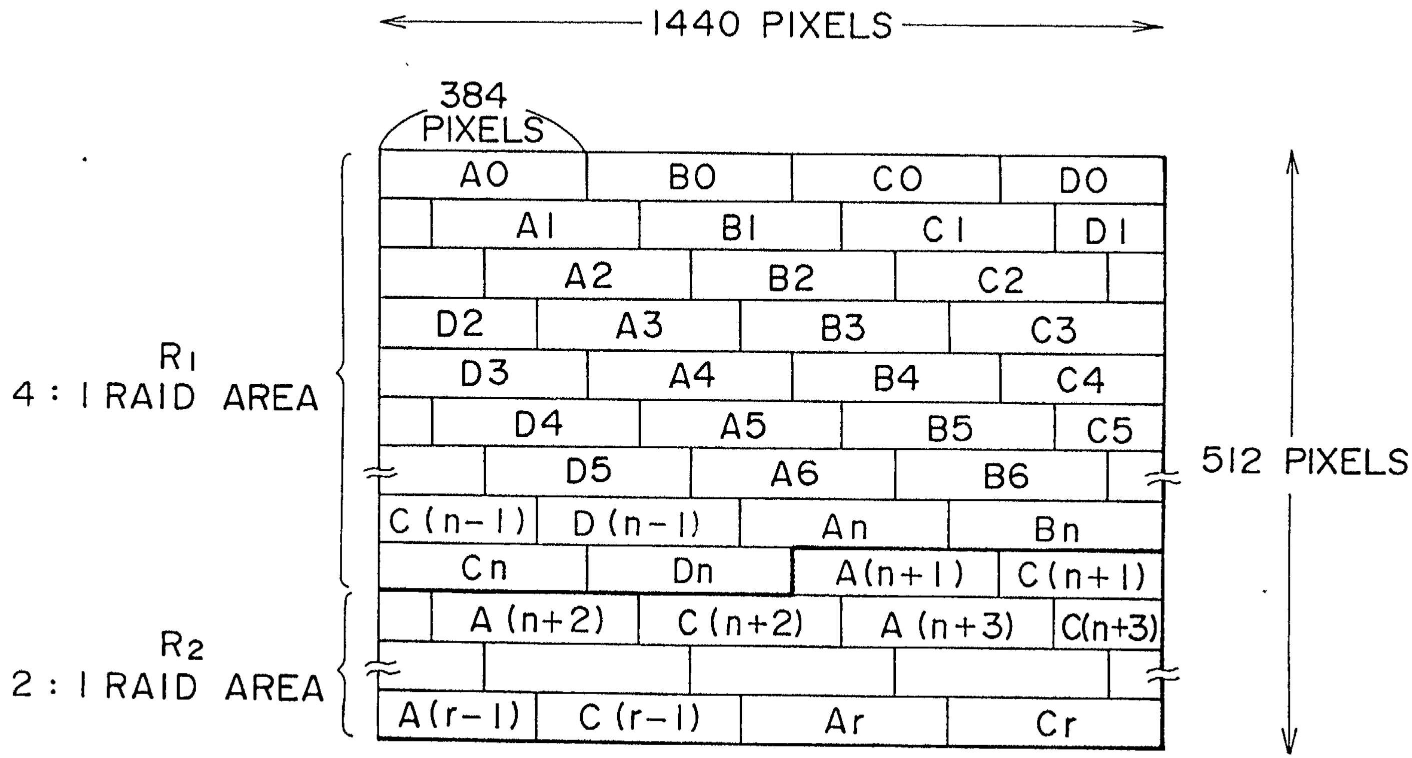

128 WORDS
(384 PIXELS)
ADDRESS
a0
A0
a0+128
A1
a0+128×2
A2
a0+128×3
A3
a0+128×(n-1)
A(n-1)
n (NUMBER OF LOOPS)
b0
B0
b0+128
B1
b0+128×2
B2
b0+128×3
B3
b0+128×(n-1)
B(n-1)
n
c0
C0
c0+128
C1
c0+128×2
C2
c0+128×3
C3
c0+128×(n-1)
C(n-1)
n
d0
D0
d0+128
D1
d0+128×2
D2
d0+128×3
D3
d0+128×(n-1)
D(n-1)
n
p0
P0
p0+128
P1
p0+128×2
P2
p0+128×3
P3
p0+128×(n-1)
P(n-1)
n
212

FIG. 43



F I G. 44

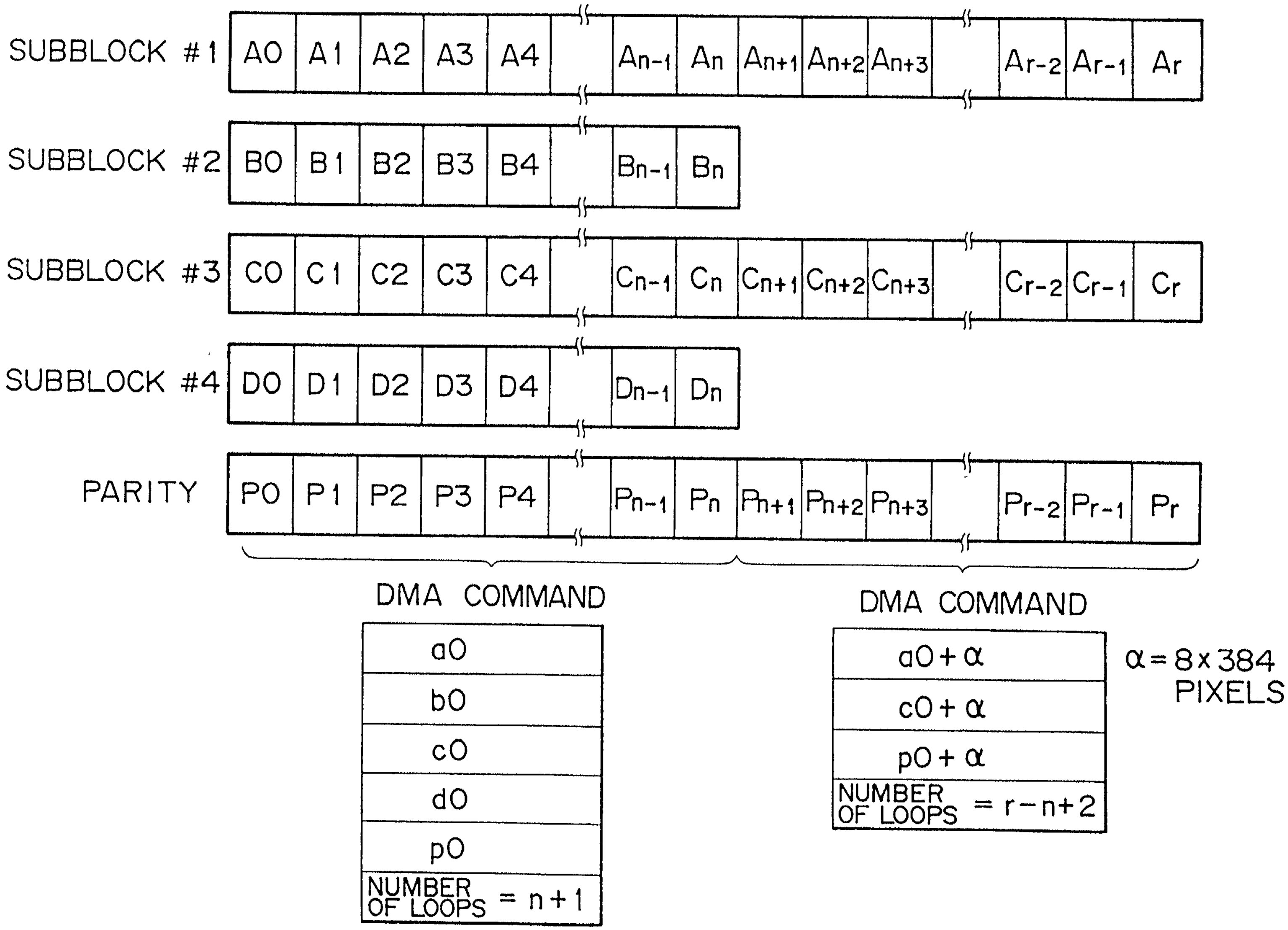

SUBBLOCK #1
A0 A1 A2 A3 A4 An-1 An An+1 An+2 An+3 Ar-2 Ar-1 Ar
SUBBLOCK #2
B0 B1 B2 B3 B4 Bn-1 Bn
SUBBLOCK #3
C0 C1 C2 C3 C4 Cn-1 Cn Cn+1 Cn+2 Cn+3 Cr-2 Cr-1 Cr
SUBBLOCK #4
D0 D1 D2 D3 D4 Dn-1 Dn
PARITY
P0 P1 P2 P3 P4 Pn-1 Pn Pn+1 Pn+2 Pn+3 Pr-2 Pr-1 Pr
DMA COMMAND
a0
b0
c0
d0
p0
NUMBER OF LOOPS = n+1
DMA COMMAND
a0+α
c0+α
p0+α
NUMBER OF LOOPS = r−n+2
α=8x384 PIXELS

FIG. 45

DMA COMMAND
(NO ERROR AT TIME OF REPRODUCTION)

a0
b0
c0
d0
NUMBER OF LOOPS

FIG. 46

DMA COMMAND
(ERROR AT TIME OF REPRODUCTION

a0
b0
p0
d0
ERROR IN NUMBER OF LOOPS C0

FIG. 47

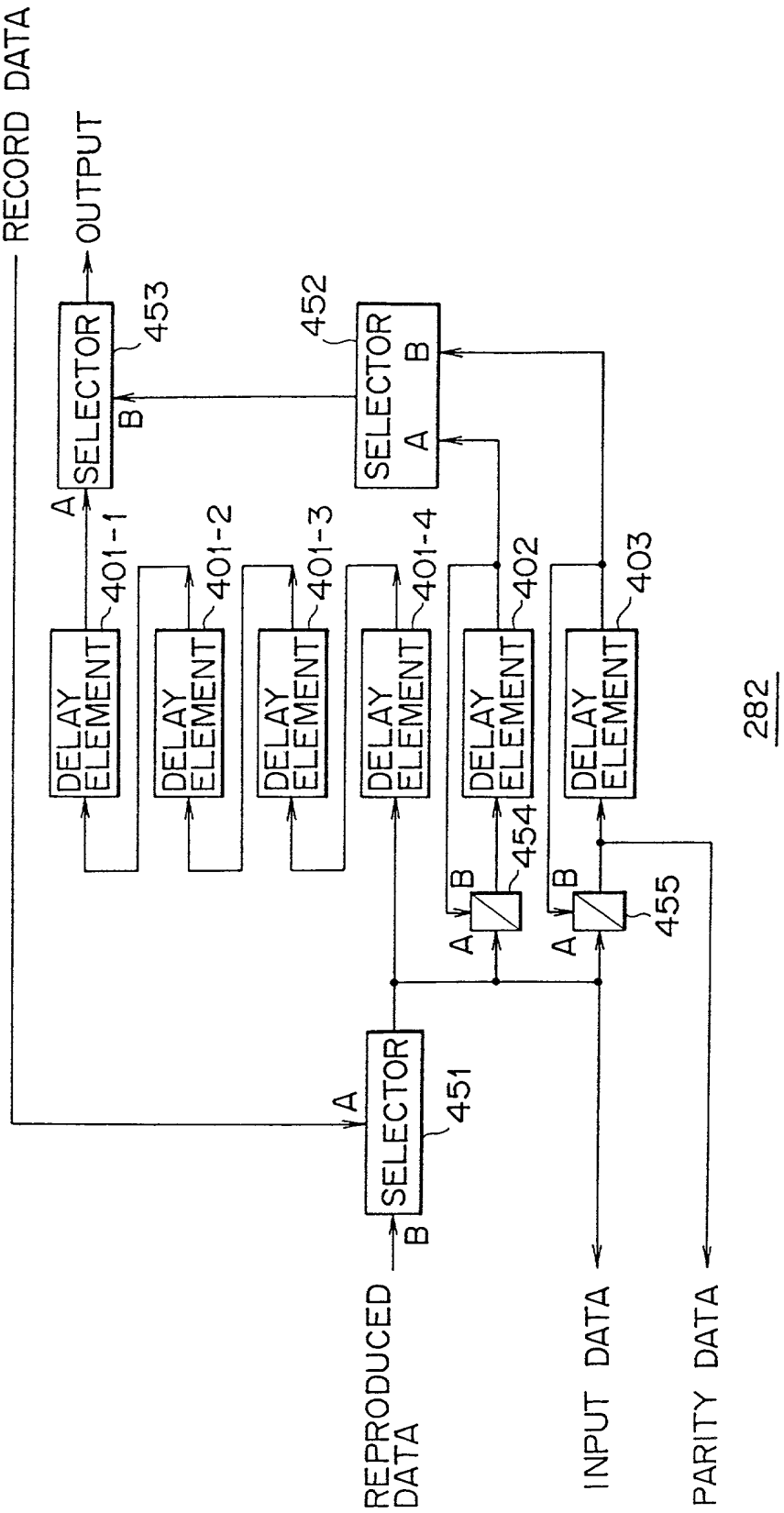

RECORD DATA
OUTPUT
SELECTOR
453
452
SELECTOR
A
B
401-1
401-2
401-3
401-4
402
403
DELAY ELEMENT
454
455
451
REPRODUCED DATA
INPUT DATA
PARITY DATA
282

FIG. 48

DATA NUMBER (PACKET TRASFER BLOCK)	0	1	2	3	4	5	6	...
SELECTOR 451	A	A	A	A	A	A	A	
SELECTOR 455	A	A^B	A^B	A^B	A	A^B	A^B	
INPUT DATA	0	1	2	3	4	5	6	
DELAY ELEMENT 403	0	0^1	0^1^2	0^1^2^3	4	4^5	4^5^6	
PARITY DATA OUTPUT	0	0^1	0^1^2	0^1^2^3	4	4^5	4^5^6	

PARITY TO BE FOUND

PARITY GENERATION

FIG. 49A

DATA NUMBER (PACKET TRASFER BLOCK)	0	1	2(P)	3
DELAY ELEMENT 401-1	—	—	—	0
DELAY ELEMENT 401-2	—	—	0	1
DELAY ELEMENT 401-3	—	0	1	2NG
DELAY ELEMENT 401-4	0	1	2NG	3
DELAY ELEMENT 402	0	0^1	0^1^P	0^1^P^3=2
DELAY ELEMENT 403	—	—	—	—
SELECTOR 452	A	A	A	A
SELECTOR 453	A	A	A	A
SELECTOR 454	A	A^B	A^B	A^B
SELECTOR 455	B	B	B	B
OUTPUT	—	—	—	—

DATA CORRECTION

FIG. 49

FIG.49A	FIG.49B

FIG.49B

4	5	6(P)	7	8	9	10
1	2NG	3	4	5	6NG	7
2NG	3	4	5	6NG	7	8
3	4	5	6NG	7	8	9
4	5	6NG	7	8	9	10
2	2	2	2	8	8^9	8^9^10
4	4^5	4^5^P	4^5^P^7=6	6	6	6
A	A	A	A	B	B	B
A	A	[B]	A	A	A	[B]
B	B	B	B	A	A^B	A^B
A	A^B	A^B	A^B	B	B	B
0	1	2 (CORECTED)	3	4	5	6 (CORECTED)

FIG.50

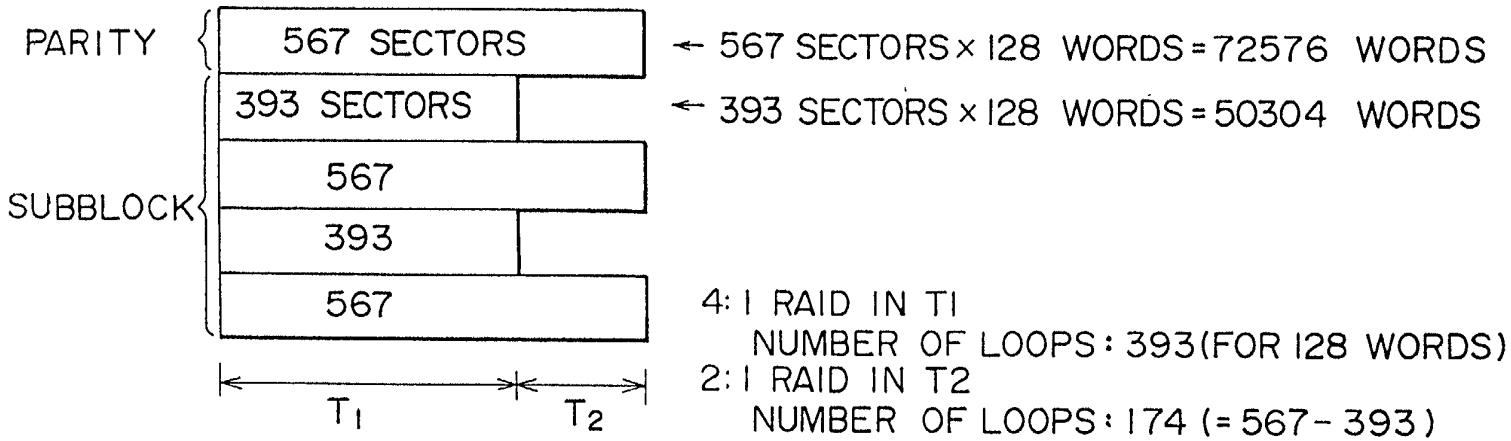

PARITY
567 SECTORS
393 SECTORS
SUBBLOCK
567
393
567
T1
T2
← 567 SECTORS × 128 WORDS = 72576 WORDS
← 393 SECTORS × 128 WORDS = 50304 WORDS
4:1 RAID IN TI
NUMBER OF LOOPS : 393 (FOR 128 WORDS)
2:1 RAID IN T2
NUMBER OF LOOPS : 174 (= 567 - 393)

FIG.51

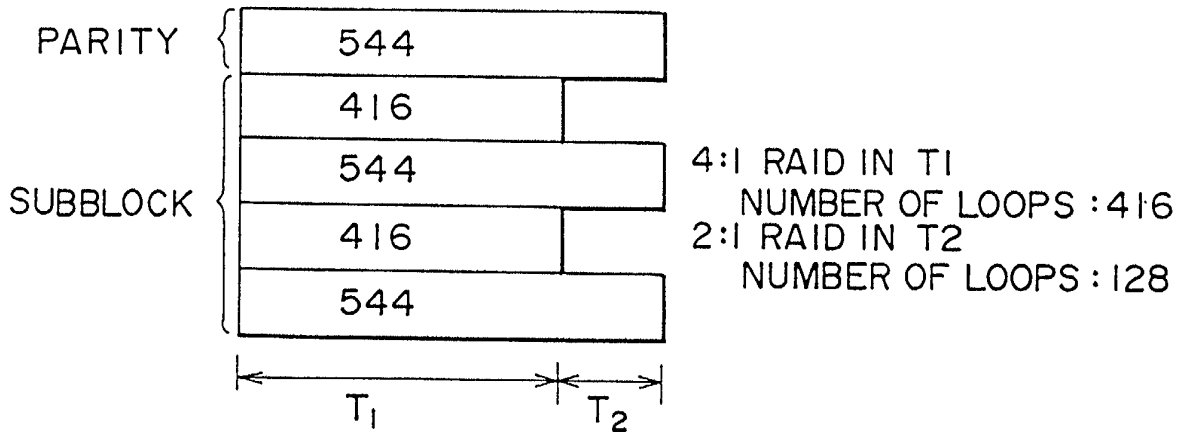

PARITY
SUBBLOCK
544
416
544
416
544
4:1 RAID IN T1
NUMBER OF LOOPS : 416
2:1 RAID IN T2
NUMBER OF LOOPS : 128
T1
T2

FIG. 52

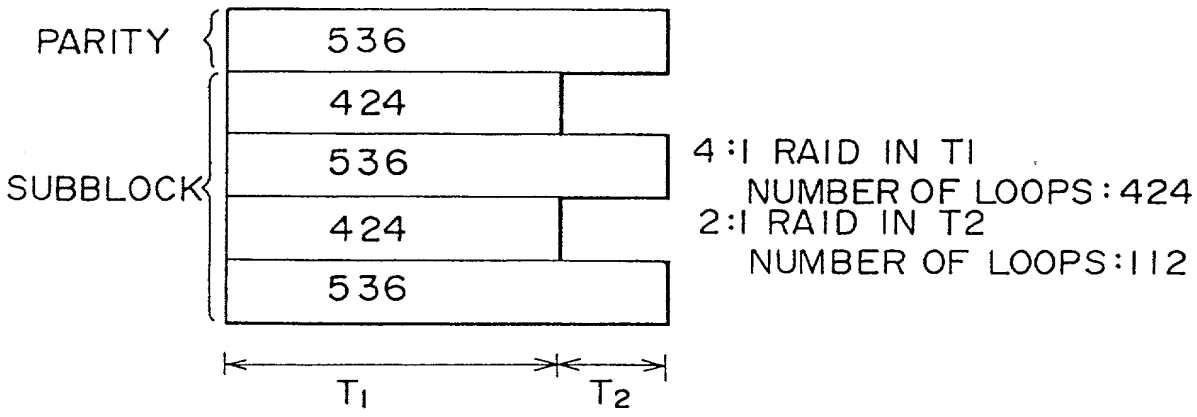

PARITY
SUBBLOCK
536
424
536
424
536
T1
T2
4:1 RAID IN TI
NUMBER OF LOOPS:424
2:1 RAID IN T2
NUMBER OF LOOPS:112

FIG. 53

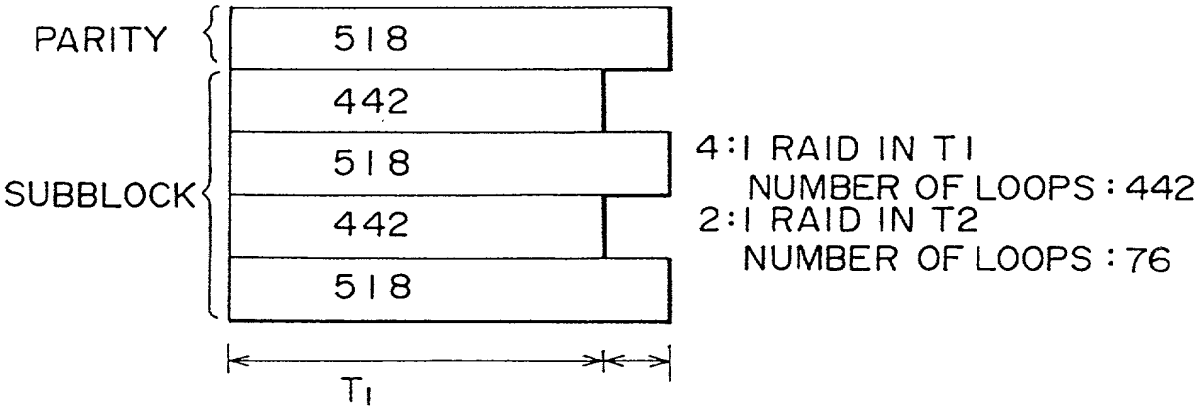

PARITY
SUBBLOCK
518
442
518
442
518
T1
4:1 RAID IN TI
NUMBER OF LOOPS:442
2:1 RAID IN T2
NUMBER OF LOOPS:76

FIG. 54

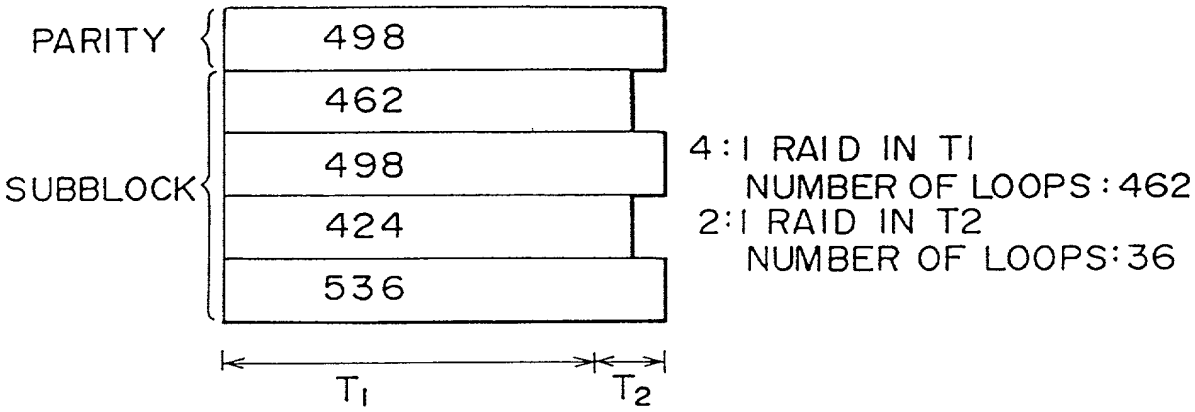

PARITY
SUBBLOCK
498
462
498
424
536
T1
T2
4:1 RAID IN TI
NUMBER OF LOOPS:462
2:1 RAID IN T2
NUMBER OF LOOPS:36

FIG. 55

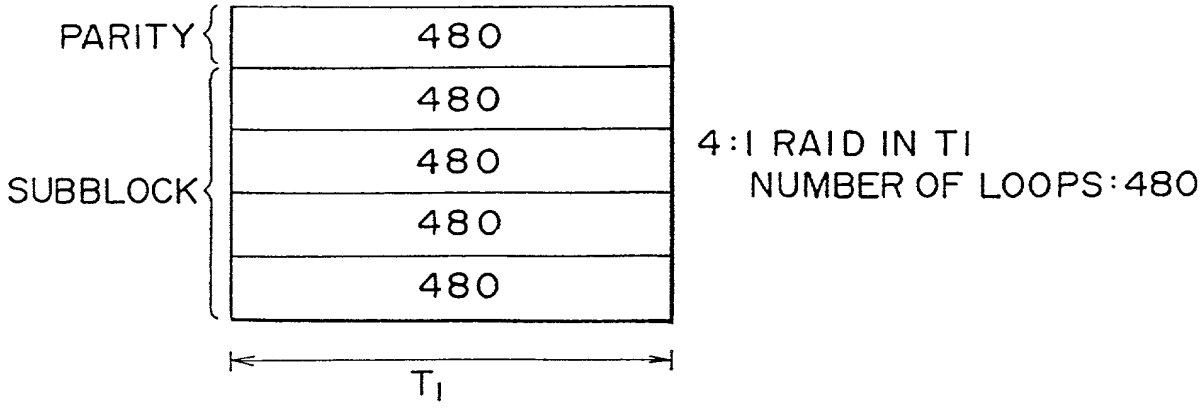
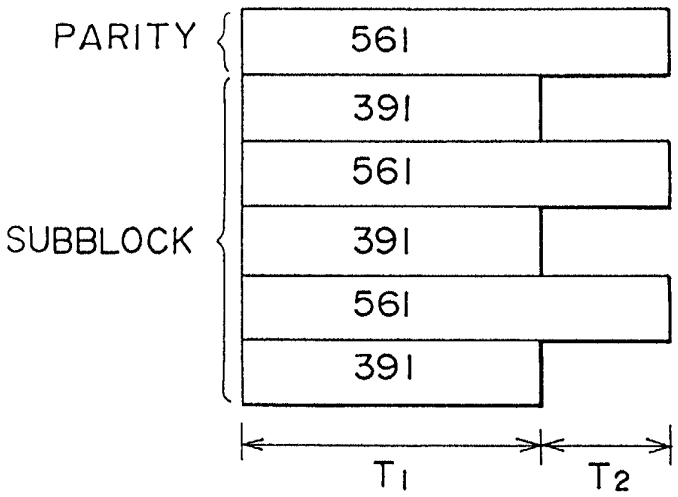

PARITY
SUBBLOCK
480
480
480
480
480
T1
4:1 RAID IN TI
NUMBER OF LOOPS:480

FIG.56



5 : 1 RAID IN T1
391 LOOPS ON 128-WORD PACKET TRANSFER
2 : 1 RAID IN T2
170 LOOPS ON 128-WORD PACKET TRANSFER

FIG. 57

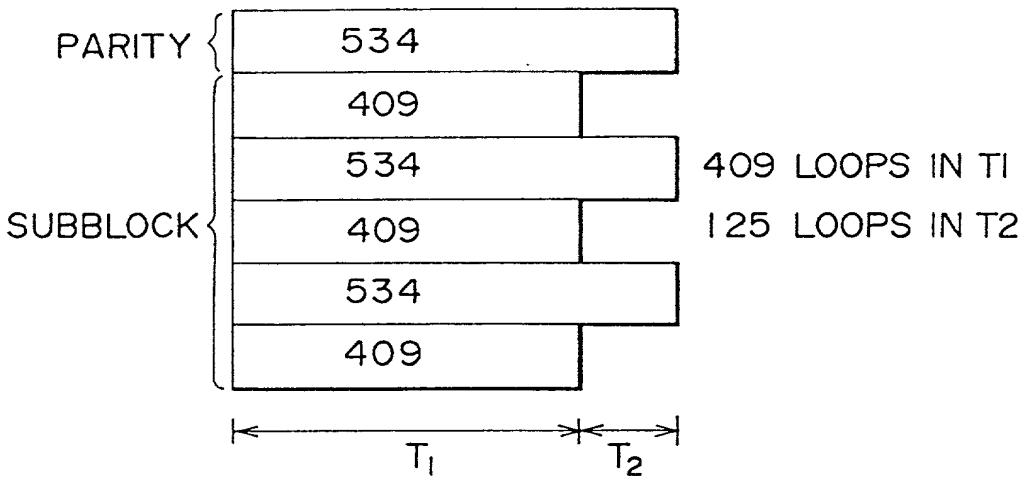

PARITY
SUBBLOCK
534
409
534
409
534
409
409 LOOPS IN TI
125 LOOPS IN T2
T1
T2

FIG. 58

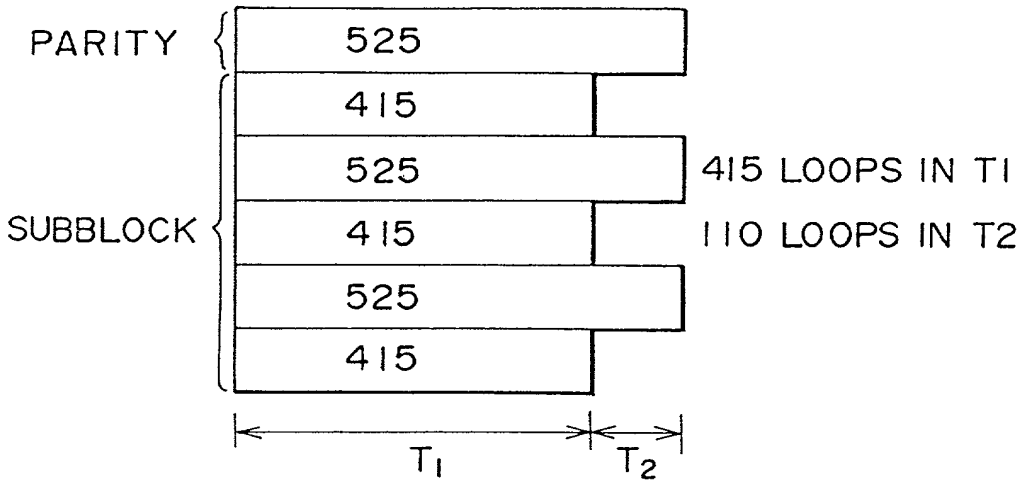

PARITY
525
415
525
415
525
415
SUBBLOCK
415 LOOPS IN T1
110 LOOPS IN T2
T1
T2

FIG. 59

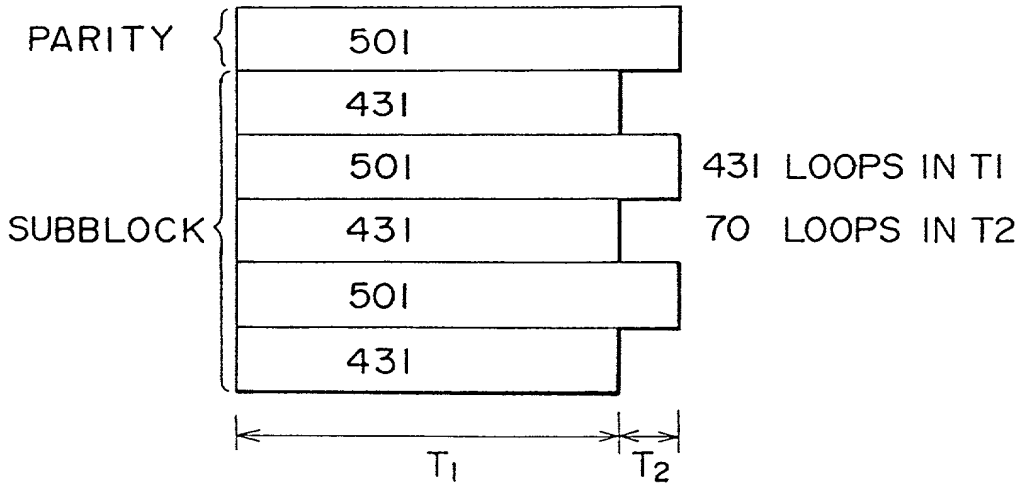

PARITY
501
431
501
431
501
431
SUBBLOCK
431 LOOPS IN T1
70 LOOPS IN T2
T1
T2

FIG. 60

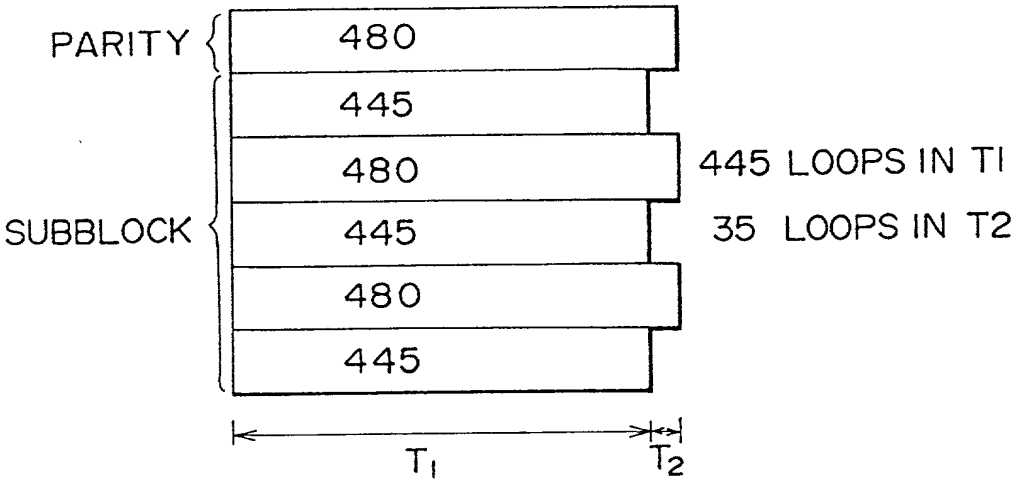

PARITY
480
445
480
445
480
445
SUBBLOCK
445 LOOPS IN TI
35 LOOPS IN T2
T1
T2

FIG. 61

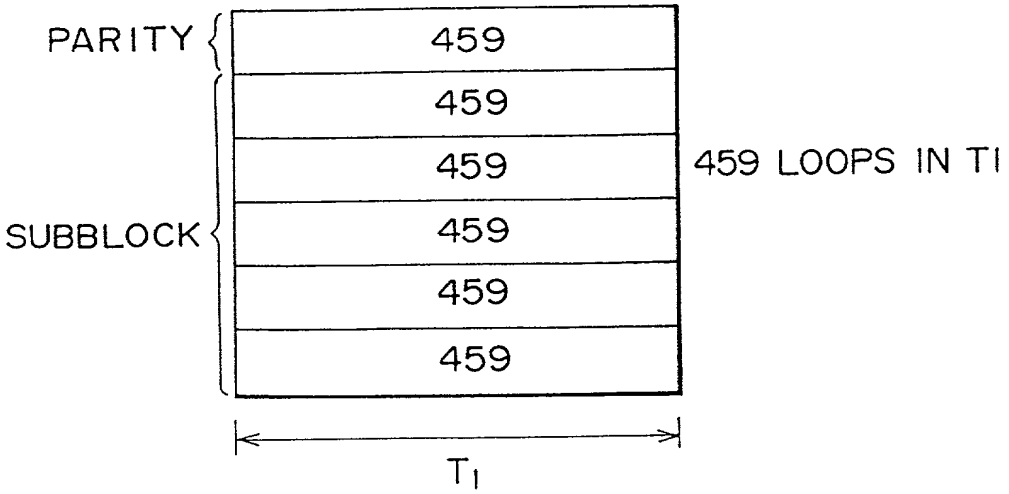

PARITY
459
459
459
459
459
459
SUBBLOCK
459 LOOPS IN TI
T1

FIG.62A

FRAME SIGNAL \ DISK ID	1	2	3
1	P1 (OUTER)	S1-1 (INNER)	S1-2 (OUTER)
2		P2 (OUTER)	S2-1 (INNER)
3	S3-4 (OUTER)		P3 (OUTER)
4	S4-3 (INNER)	S4-4 (OUTER)	
5	S5-2 (OUTER)	S5-3 (INNER)	S5-4 (OUTER)
6	S6-1 (INNER)	S6-2 (OUTER)	S6-3 (INNER)
7	P7 (OUTER)	S7-1 (INNER)	S7-2 (OUTER)
8		P8 (OUTER)	S8-1 (INNER)
9	S9-4 (OUTER)		P9 (OUTER)
10	S10-3 (OUTER)	S10-4 (OUTER)	
	.	.	.
	.	.	.
	.	.	.

FIG.62

FIG.62A	FIG.62B

F I G. 62B

4	5	6
S1 3(INNER)	S1-4(OUTER)	
S2 2(OUTER)	S2-3(INNER)	S2-4(OUTER)
S3 1(INNER)	S3-2(OUTER)	S3-3(INNER)
P4 (OUTER)	S4-1(INNER)	S4-2(OUTER)
	P5 (OUTER)	S5-1(INNER)
S6 4(OUTER)		P6 (OUTER)
S7 3(INNER)	S7-4(OUTER)	
S8 2(OUTER)	S8-3(INNER)	S8-4(OUTER
S9 1(INNER)	S9-2(OUTER)	S9-3(INNER)
P10 (OUTER)	S10-1	S10-2(OUTER)
⋮	⋮	⋮

FIG. 63

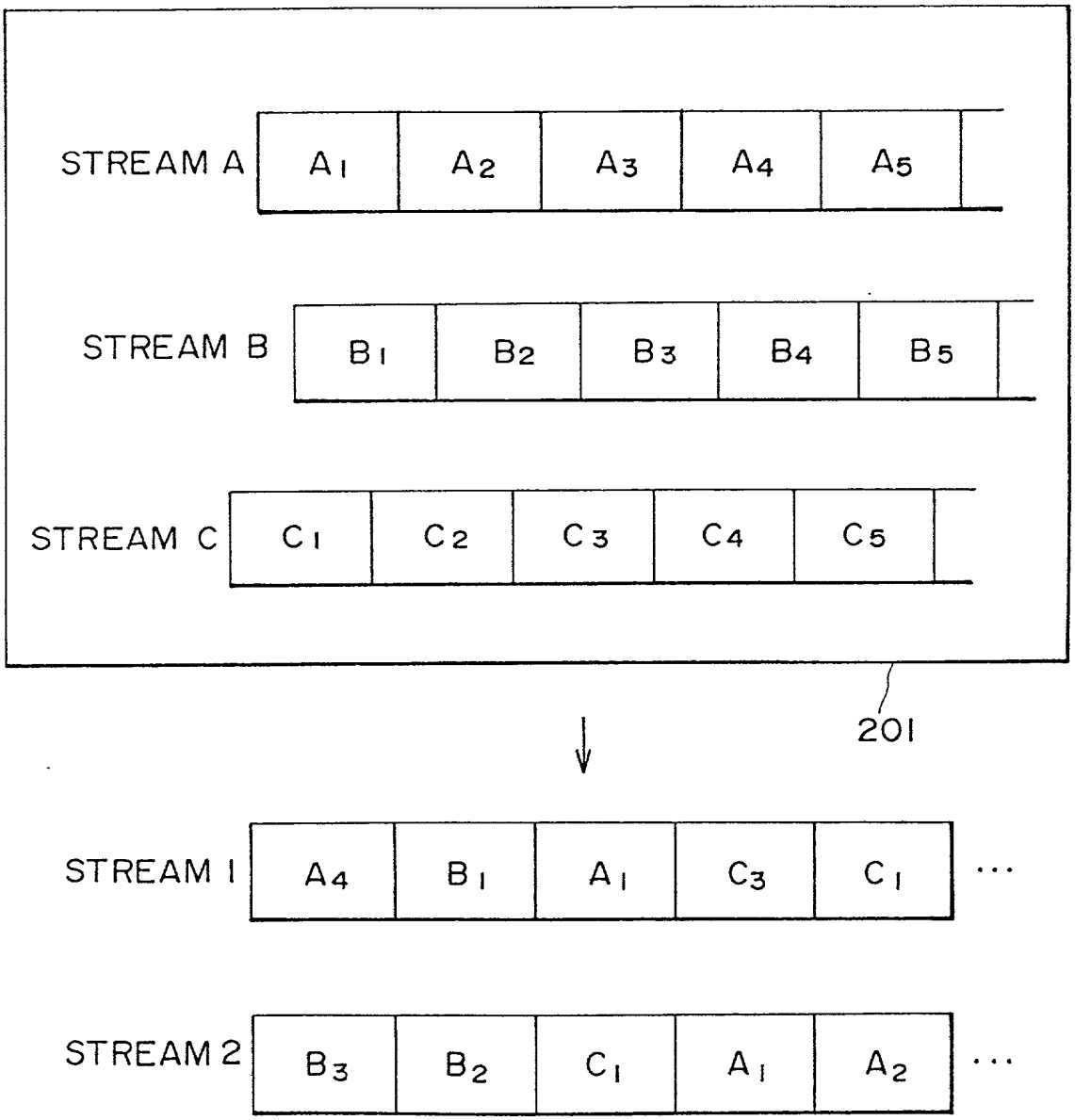

STREAM A
A1
A2
A3
A4
A5
STREAM B
B1
B2
B3
B4
B5
STREAM C
C1
C2
C3
C4
C5
201
STREAM 1
A4
B1
A1
C3
C1
...
STREAM 2
B3
B2
C1
A1
A2
...

FIG. 64

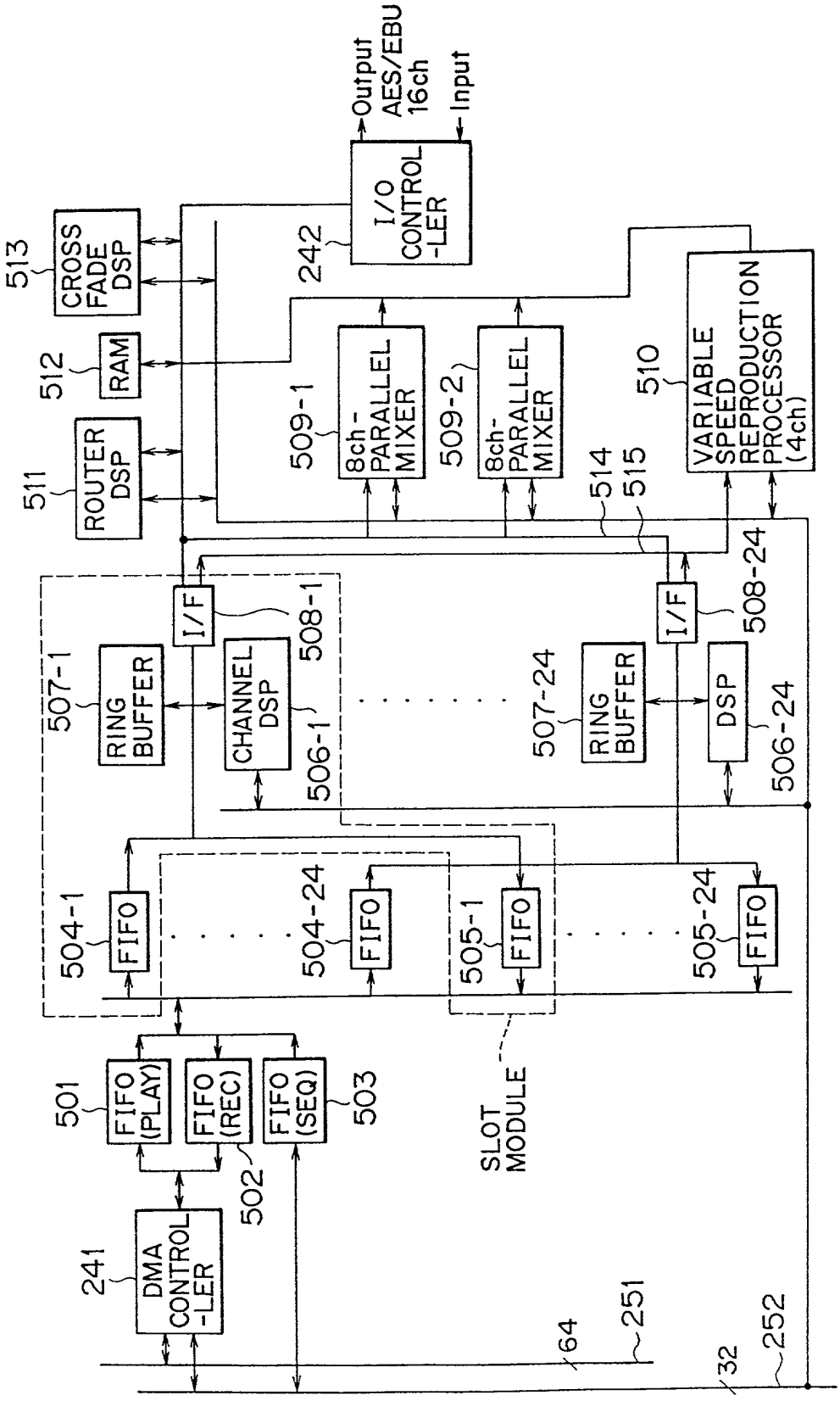

241
DMA CONTROL -LER
501
FIFO (PLAY)
FIFO (REC)
502
FIFO (SEQ)
503
504-1
FIFO
504-24
505-1
505-24
SLOT MODULE
507-1
RING BUFFER
507-24
508-1
CHANNEL DSP
506-1
508-24
DSP
506-24
I/F
509-1
8ch-PARALLEL MIXER
509-2
510
VARIABLE SPEED REPRODUCTION PROCESSOR (4ch)
511
ROUTER DSP
512
RAM
513
CROSS FADE DSP
514
515
242
I/O CONTROL -LER
Output AES/EBU 16ch
Input
64
251
32
252
231

FIG. 65A

FIG. 65B

FIG. 65C

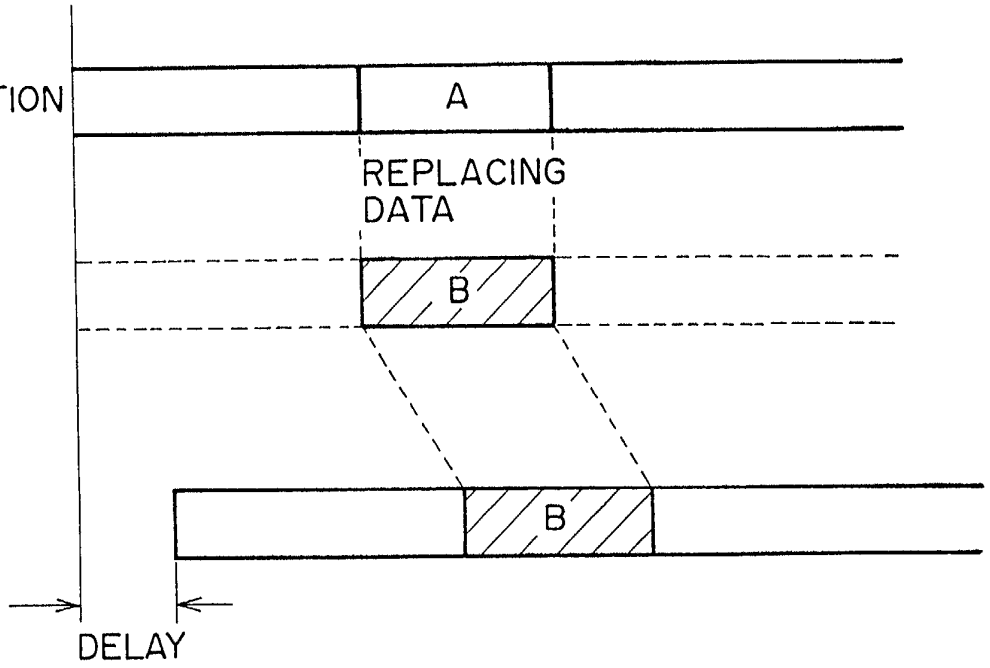


FIG. 66

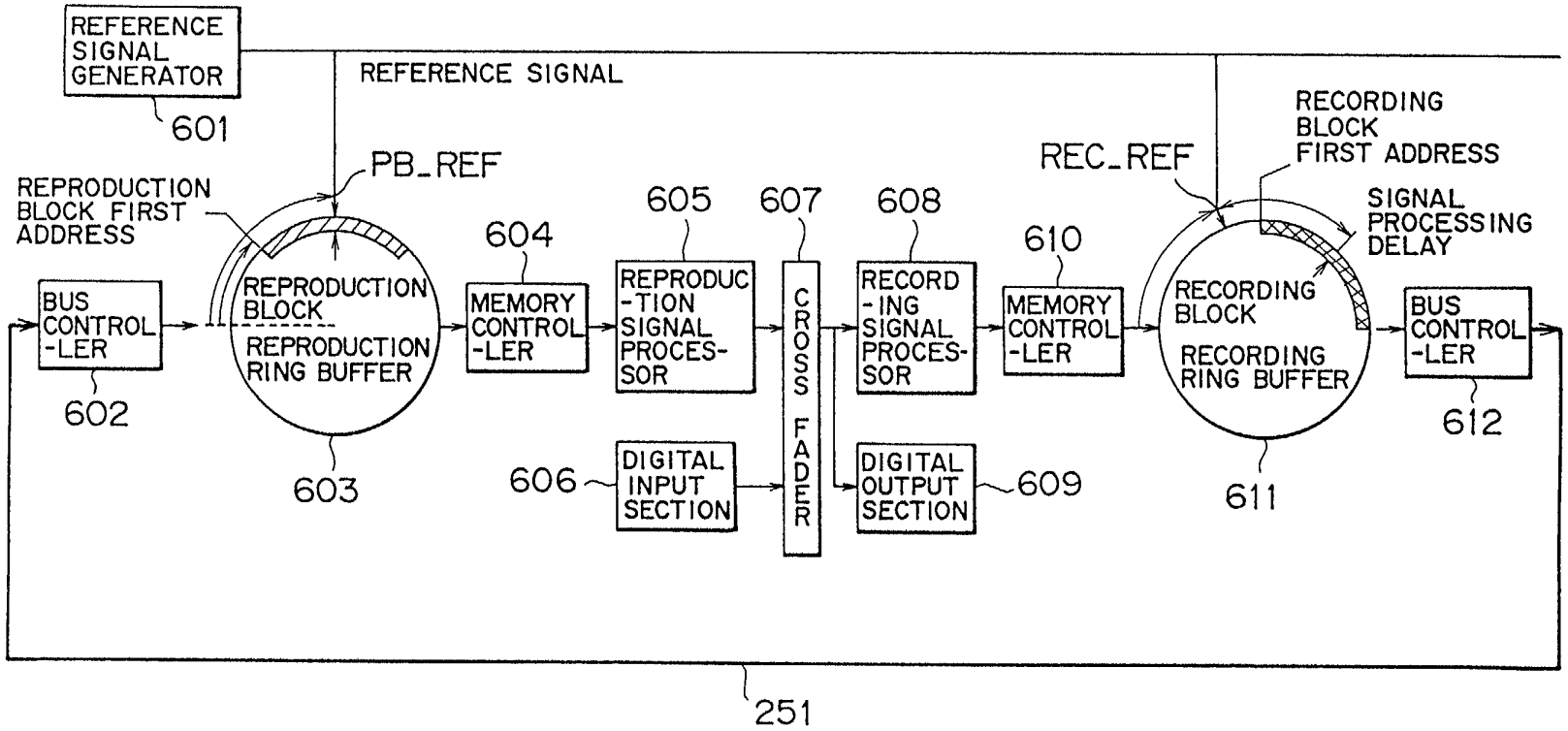

REFERENCE SIGNAL GENERATOR
601
REFERENCE SIGNAL
PB_REF
REPRODUCTION BLOCK FIRST ADDRESS
REC_REF
RECORDING BLOCK FIRST ADDRESS
SIGNAL PROCESSING DELAY
BUS CONTROL -LER
602
REPRODUCTION BLOCK
REPRODUCTION RING BUFFER
603
MEMORY CONTROL -LER
604
REPRODUC -TION SIGNAL PROCES- SOR
605
DIGITAL INPUT SECTION
606
CROSS FADER
607
RECORD -ING SIGNAL PROCES- SOR
608
DIGITAL OUTPUT SECTION
609
MEMORY CONTROL -LER
610
RECORDING BLOCK
RECORDING RING BUFFER
611
BUS CONTROL -LER
612
251

FIG.67

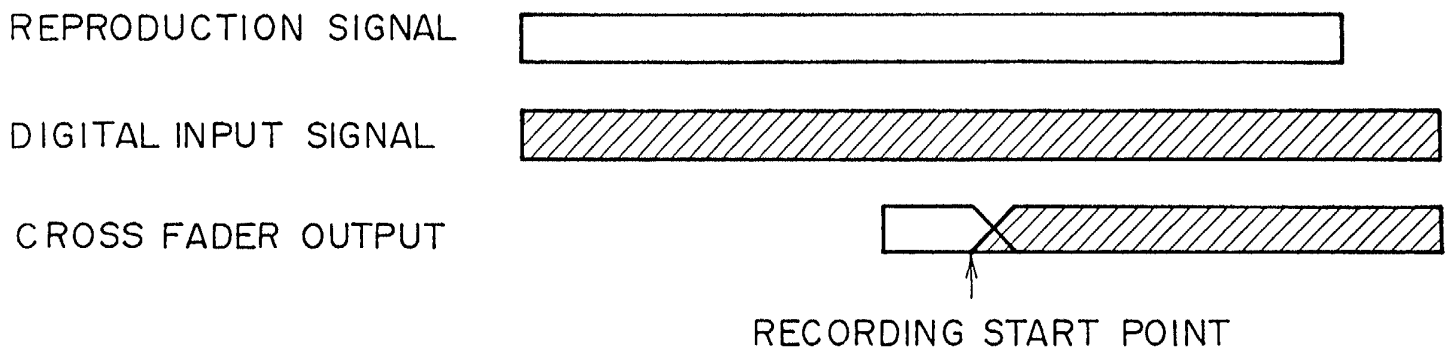

REPRODUCTION SIGNAL
DIGITAL INPUT SIGNAL
CROSS FADER OUTPUT
RECORDING START POINT

FIG. 68

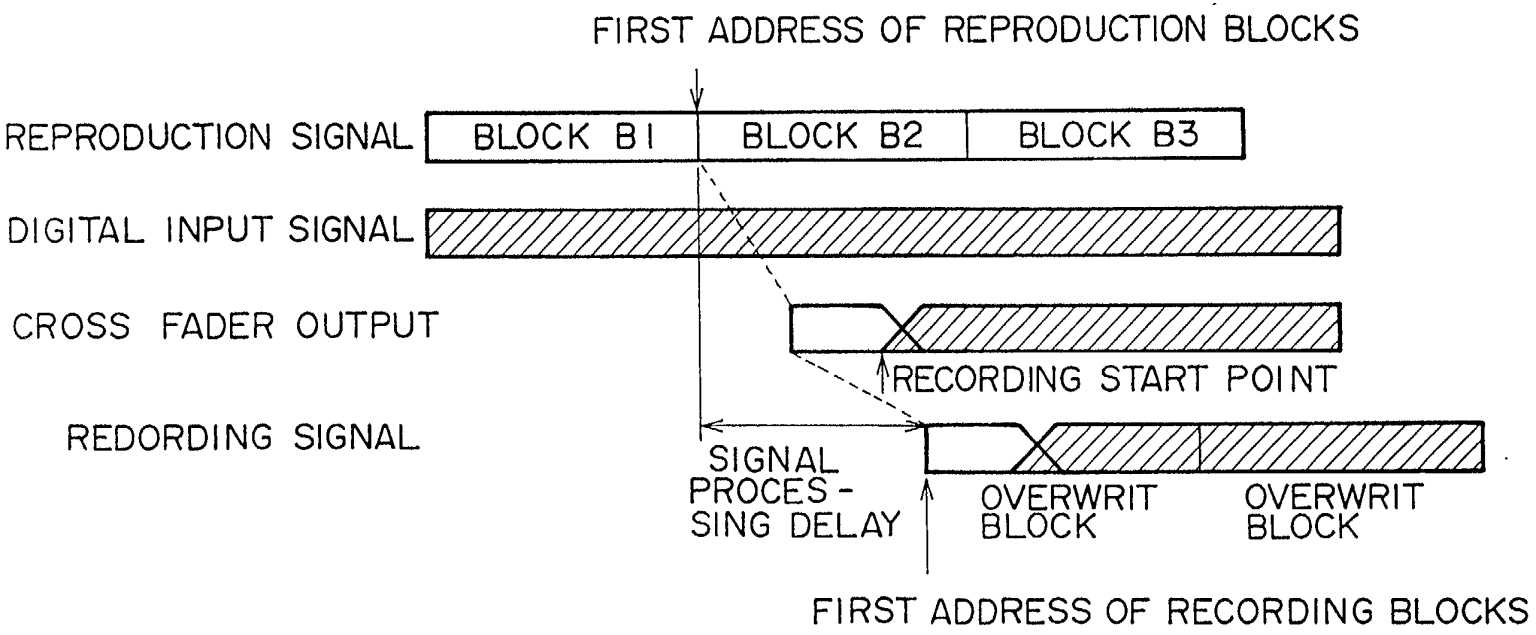

FIRST ADDRESS OF REPRODUCTION BLOCKS
REPRODUCTION SIGNAL
BLOCK B1
BLOCK B2
BLOCK B3
DIGITAL INPUT SIGNAL
CROSS FADER OUTPUT
RECORDING START POINT
REDORDING SIGNAL
SIGNAL PROCES-SING DELAY
OVERWRIT BLOCK
OVERWRIT BLOCK
FIRST ADDRESS OF RECORDING BLOCKS

FIG. 69

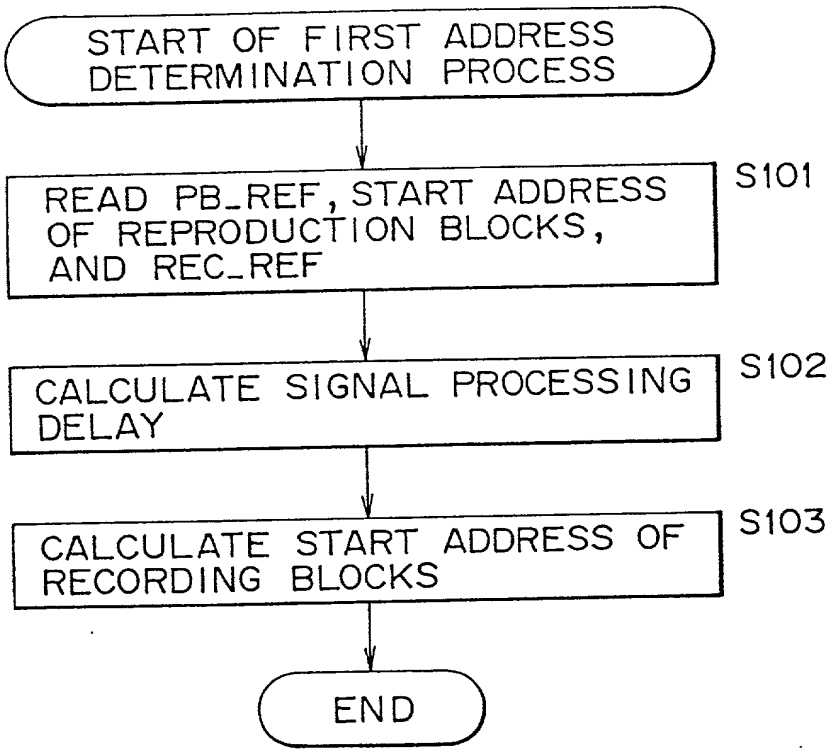

START OF FIRST ADDRESS DETERMINATION PROCESS
READ PB_REF, START ADDRESS OF REPRODUCTION BLOCKS, AND REC_REF
S101
CALCULATE SIGNAL PROCESSING DELAY
S102
CALCULATE START ADDRESS OF RECORDING BLOCKS
S103
END

FIG. 70

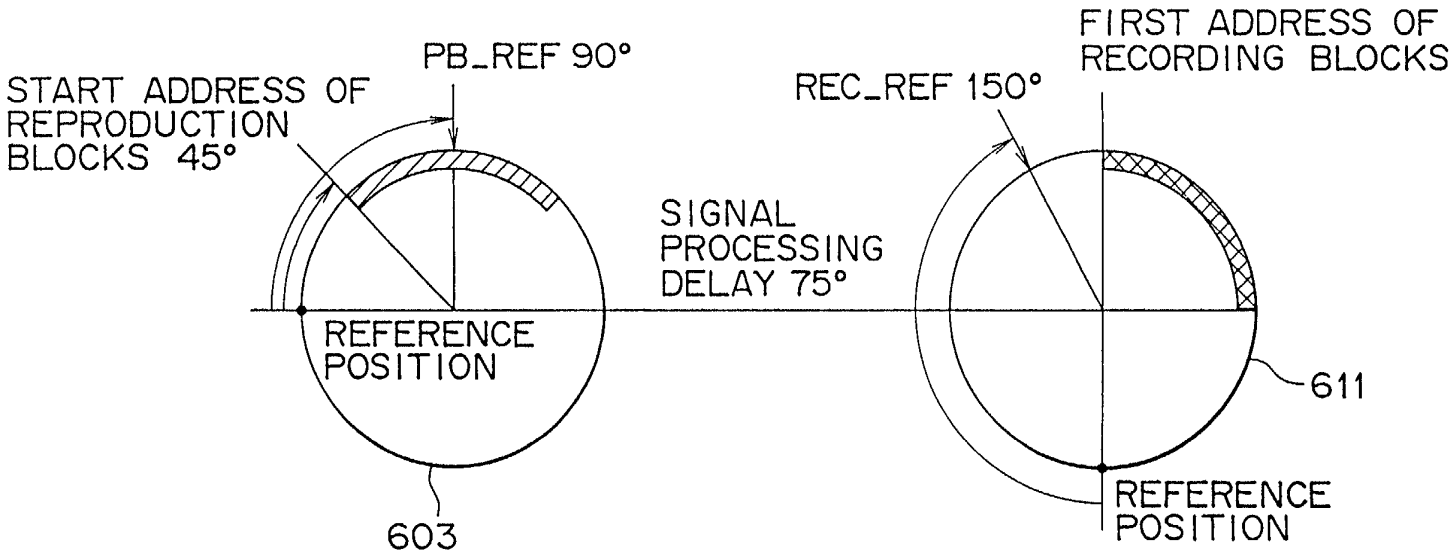
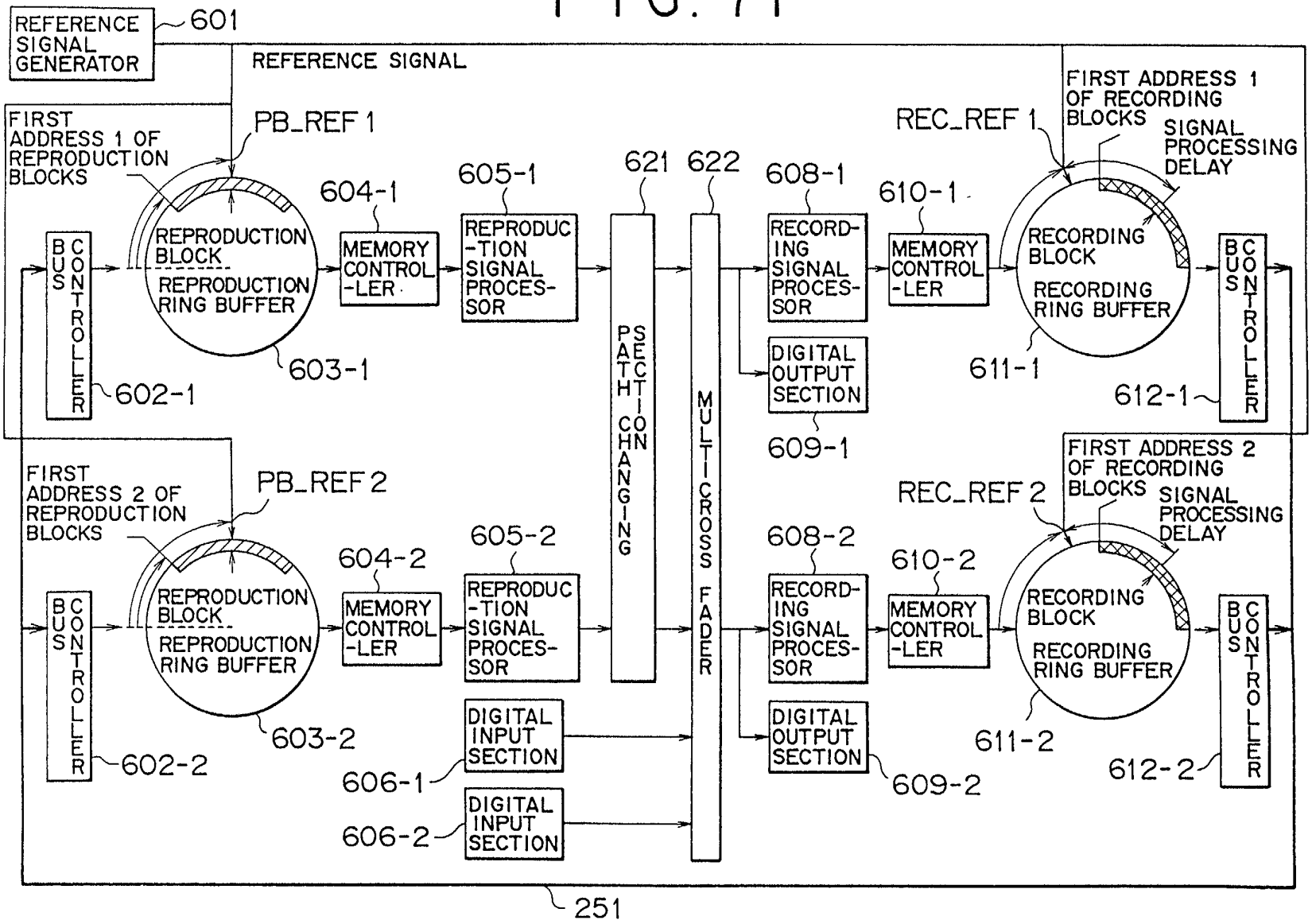

START ADDRESS OF
REPRODUCTION
BLOCKS 45°
PB_REF 90°
REFERENCE
POSITION
603
SIGNAL
PROCESSING
DELAY 75°
REC_REF 150°
FIRST ADDRESS OF
RECORDING BLOCKS
611
REFERENCE
POSITION

FIG. 71


REFERENCE SIGNAL GENERATOR
601
REFERENCE SIGNAL
FIRST ADDRESS 1 OF REPRODUCTION BLOCKS
PB_REF 1
REPRODUCTION BLOCK
REPRODUCTION RING BUFFER
603-1
BUS CONTROLLER
602-1
604-1
MEMORY CONTROL-LER
605-1
REPRODUC-TION SIGNAL PROCES-SOR
621
622
PATH SECTION CHANGING
MULTICROSS FADER
608-1
RECORD-ING SIGNAL PROCES-SOR
DIGITAL OUTPUT SECTION
609-1
610-1
MEMORY CONTROL-LER
REC_REF 1
FIRST ADDRESS 1 OF RECORDING BLOCKS
SIGNAL PROCESSING DELAY
RECORDING BLOCK
RECORDING RING BUFFER
611-1
BUS CONTROLLER
612-1
FIRST ADDRESS 2 OF REPRODUCTION BLOCKS
PB_REF 2
REPRODUCTION BLOCK
REPRODUCTION RING BUFFER
603-2
BUS CONTROLLER
602-2
604-2
MEMORY CONTROL-LER
605-2
REPRODUC-TION SIGNAL PROCES-SOR
DIGITAL INPUT SECTION
606-1
DIGITAL INPUT SECTION
606-2
608-2
RECORD-ING SIGNAL PROCES-SOR
DIGITAL OUTPUT SECTION
609-2
610-2
MEMORY CONTROL-LER
REC_REF 2
FIRST ADDRESS 2 OF RECORDING BLOCKS
SIGNAL PROCESSING DELAY
RECORDING BLOCK
RECORDING RING BUFFER
611-2
BUS CONTROLLER
612-2
251

F I G. 72

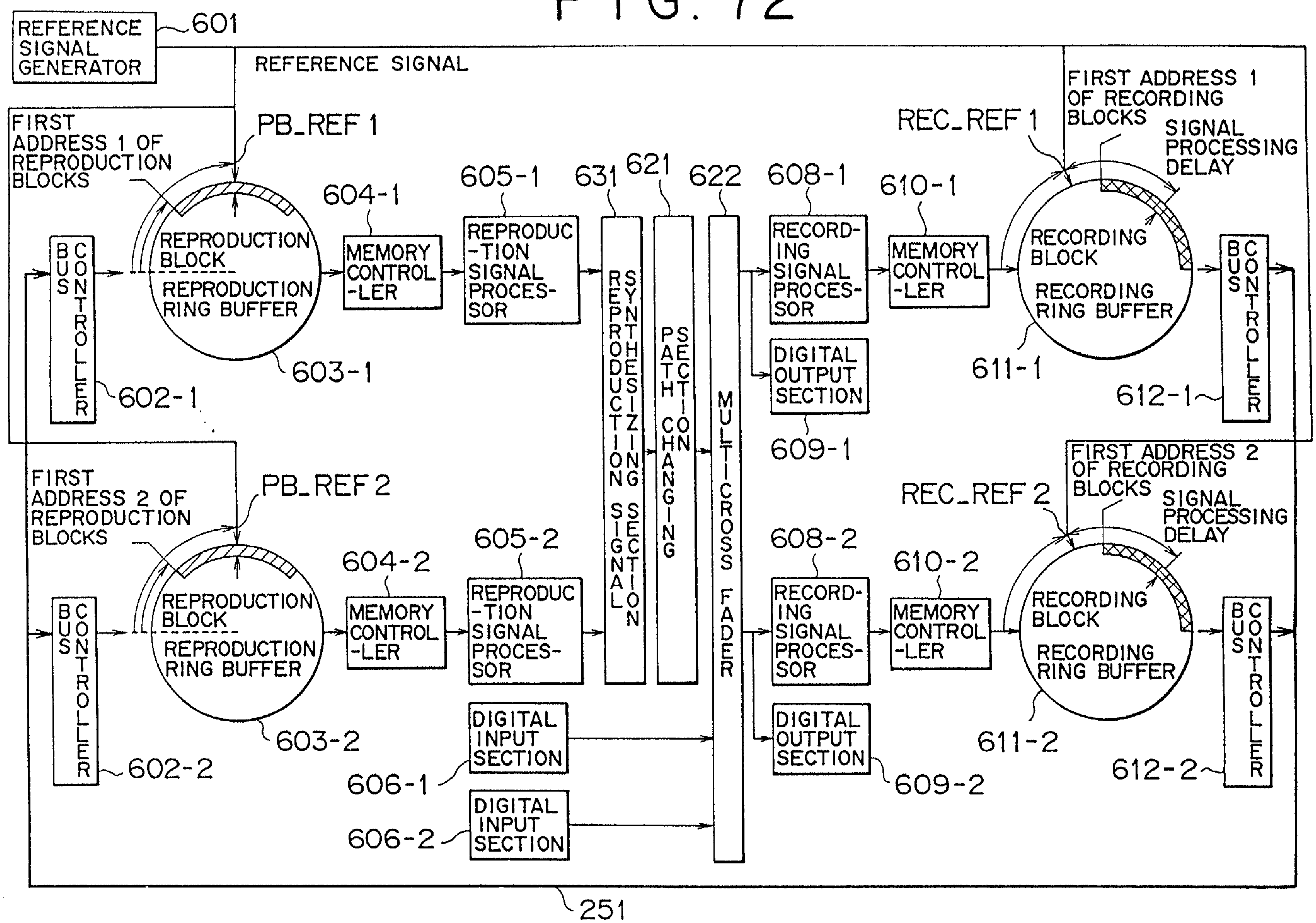

REFERENCE SIGNAL GENERATOR
601
REFERENCE SIGNAL
FIRST ADDRESS 1 OF REPRODUCTION BLOCKS
PB_REF 1
BUS CONTROLLER
602-1
REPRODUCTION BLOCK
REPRODUCTION RING BUFFER
603-1
604-1
MEMORY CONTROL-LER
605-1
REPRODUC-TION SIGNAL PROCES-SOR
631
REPRODUCTION SIGNAL SYNTHESIZING SECTION
621
PATH CHANGING SECTION
622
MULTICROSS FADER
608-1
RECORD-ING SIGNAL PROCES-SOR
DIGITAL OUTPUT SECTION
609-1
610-1
MEMORY CONTROL-LER
REC_REF 1
FIRST ADDRESS 1 OF RECORDING BLOCKS
SIGNAL PROCESSING DELAY
RECORDING BLOCK
RECORDING RING BUFFER
611-1
BUS CONTROLLER
612-1
FIRST ADDRESS 2 OF REPRODUCTION BLOCKS
PB_REF 2
BUS CONTROLLER
602-2
REPRODUCTION BLOCK
REPRODUCTION RING BUFFER
603-2
604-2
MEMORY CONTROL-LER
605-2
REPRODUC-TION SIGNAL PROCES-SOR
DIGITAL INPUT SECTION
606-1
DIGITAL INPUT SECTION
606-2
608-2
RECORD-ING SIGNAL PROCES-SOR
DIGITAL OUTPUT SECTION
609-2
610-2
MEMORY CONTROL-LER
REC_REF 2
FIRST ADDRESS 2 OF RECORDING BLOCKS
SIGNAL PROCESSING DELAY
RECORDING BLOCK
RECORDING RING BUFFER
611-2
BUS CONTROLLER
612-2
251

FIG. 73

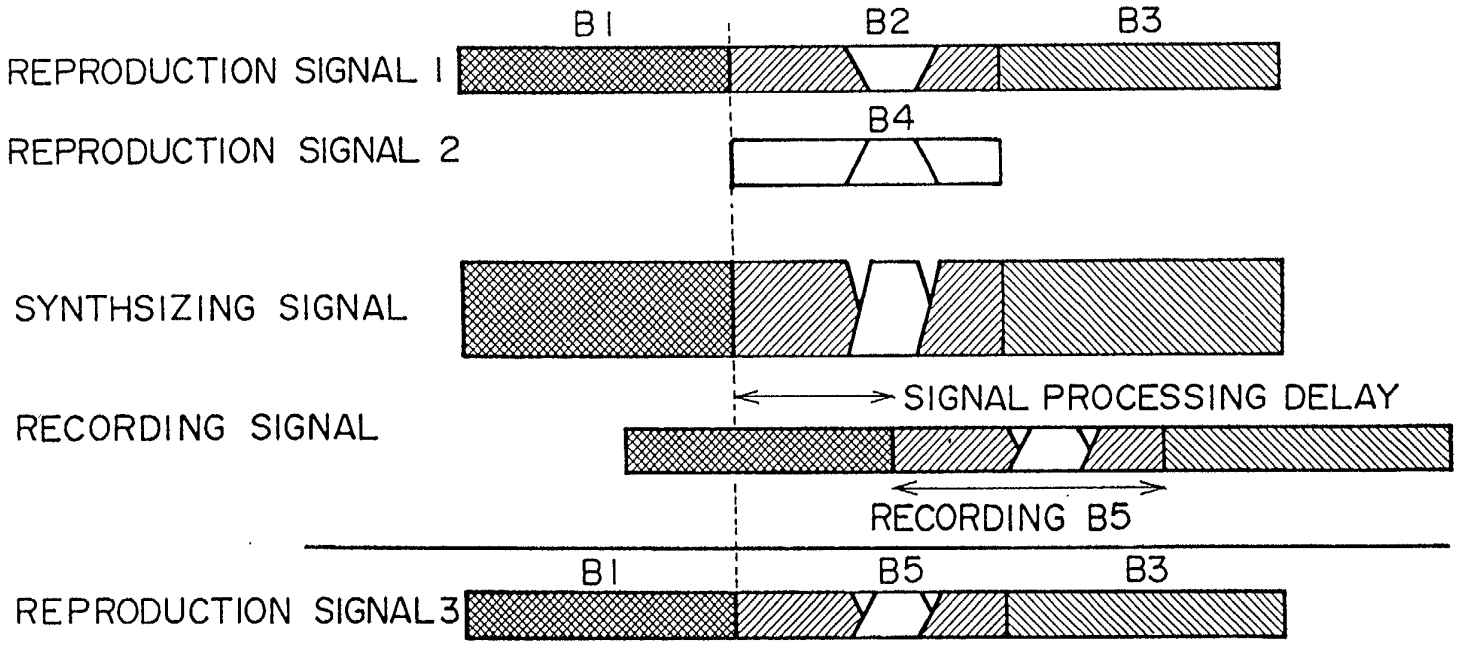

B1
B2
B3
REPRODUCTION SIGNAL 1
B4
REPRODUCTION SIGNAL 2
SYNTHSIZING SIGNAL
SIGNAL PROCESSING DELAY
RECORDING SIGNAL
RECORDING B5
B1
B5
B3
REPRODUCTION SIGNAL3

FIG. 74

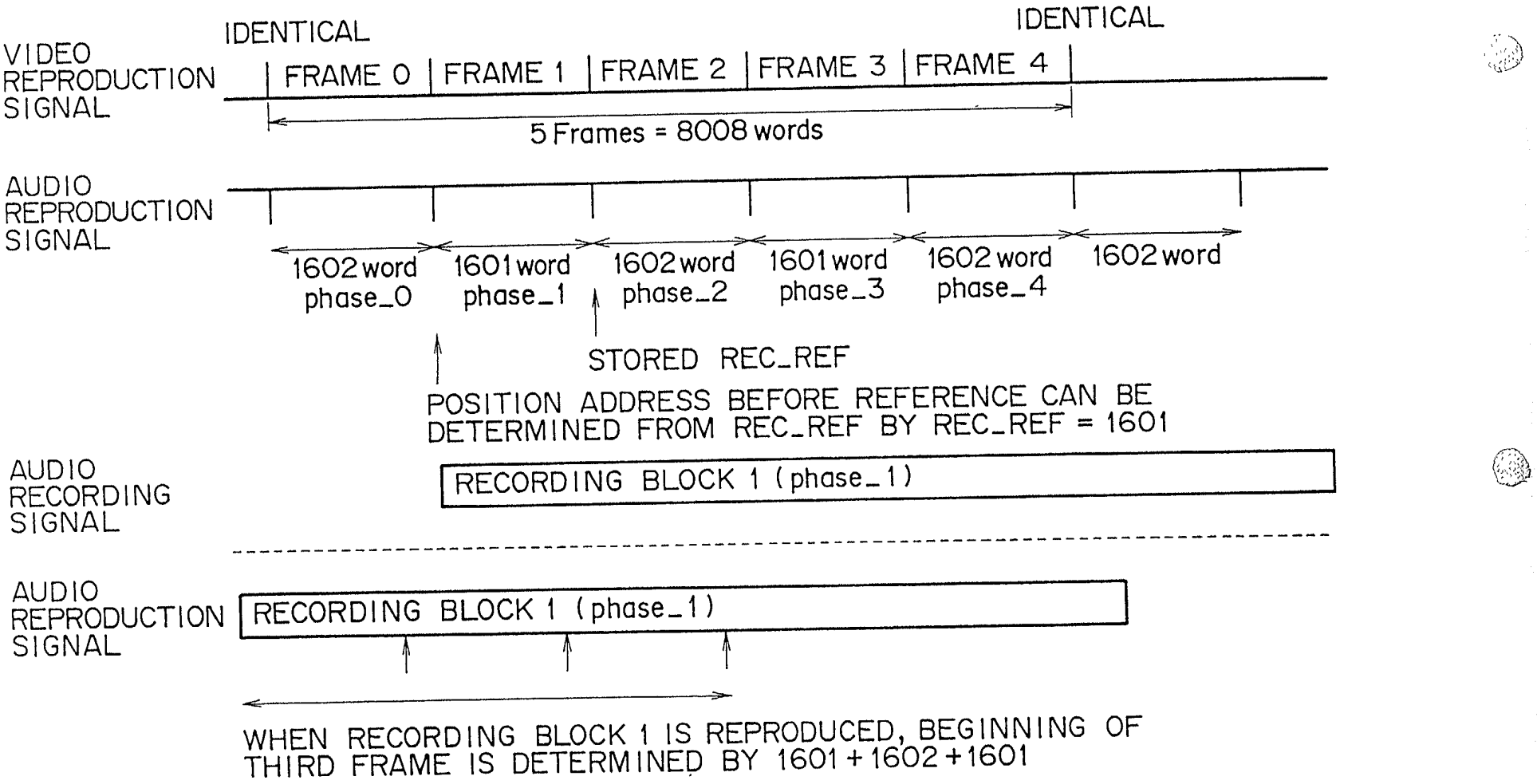

IDENTICAL
IDENTICAL
VIDEO REPRODUCTION SIGNAL
FRAME 0
FRAME 1
FRAME 2
FRAME 3
FRAME 4
5 Frames = 8008 words
AUDIO REPRODUCTION SIGNAL
1602 word phase_0
1601 word phase_1
1602 word phase_2
1601 word phase_3
1602 word phase_4
1602 word
STORED REC_REF
POSITION ADDRESS BEFORE REFERENCE CAN BE DETERMINED FROM REC_REF BY REC_REF = 1601
AUDIO RECORDING SIGNAL
RECORDING BLOCK 1 (phase_1)
AUDIO REPRODUCTION SIGNAL
RECORDING BLOCK 1 (phase_1)
WHEN RECORDING BLOCK 1 IS REPRODUCED, BEGINNING OF THIRD FRAME IS DETERMINED BY 1601 + 1602 + 1601

FIG. 75A

FIG. 75B

FIG. 75C

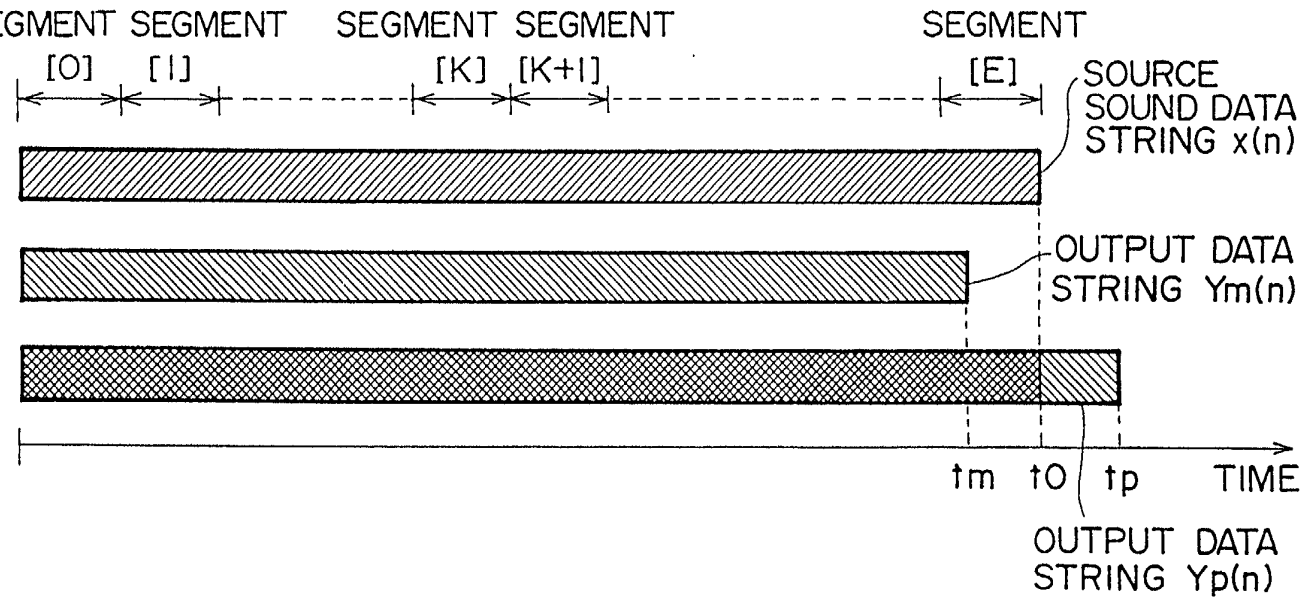


FIG. 76

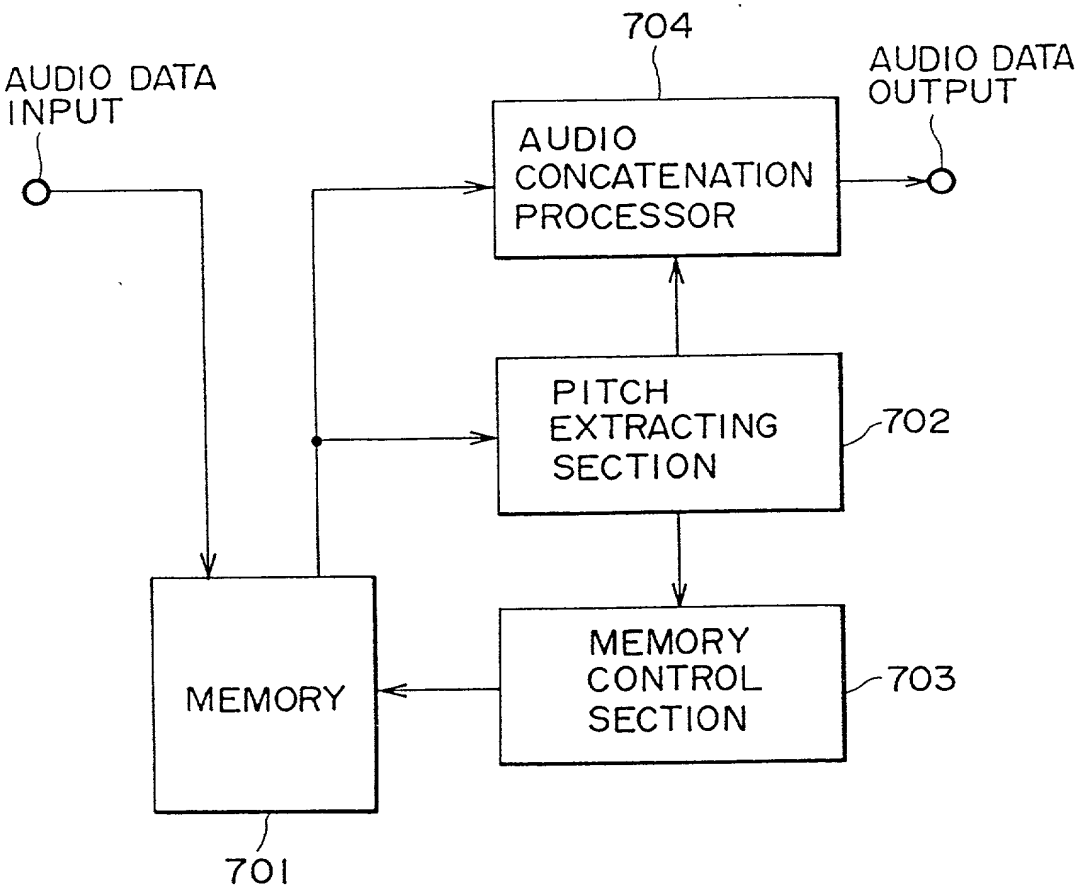

704
AUDIO DATA INPUT
AUDIO DATA OUTPUT
AUDIO CONCATENATION PROCESSOR
PITCH EXTRACTING SECTION
702
MEMORY
MEMORY CONTROL SECTION
703
701

FIG. 77

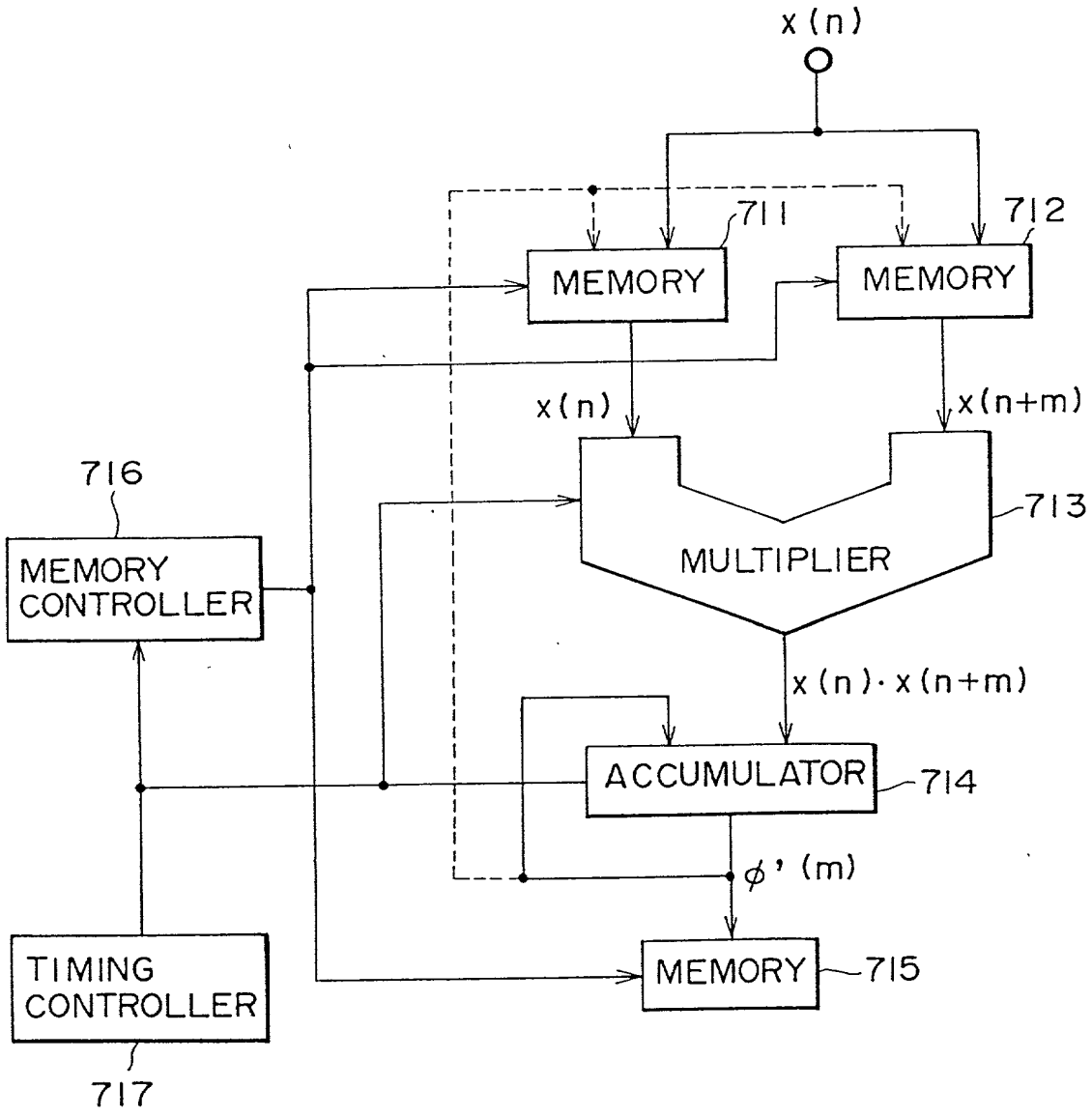

x(n)
711
712
MEMORY
MEMORY
x(n)
x(n+m)
716
713
MEMORY CONTROLLER
MULTIPLIER
x(n)·x(n+m)
ACCUMULATOR
714
φ'(m)
TIMING CONTROLLER
MEMORY
715
717

FIG. 78

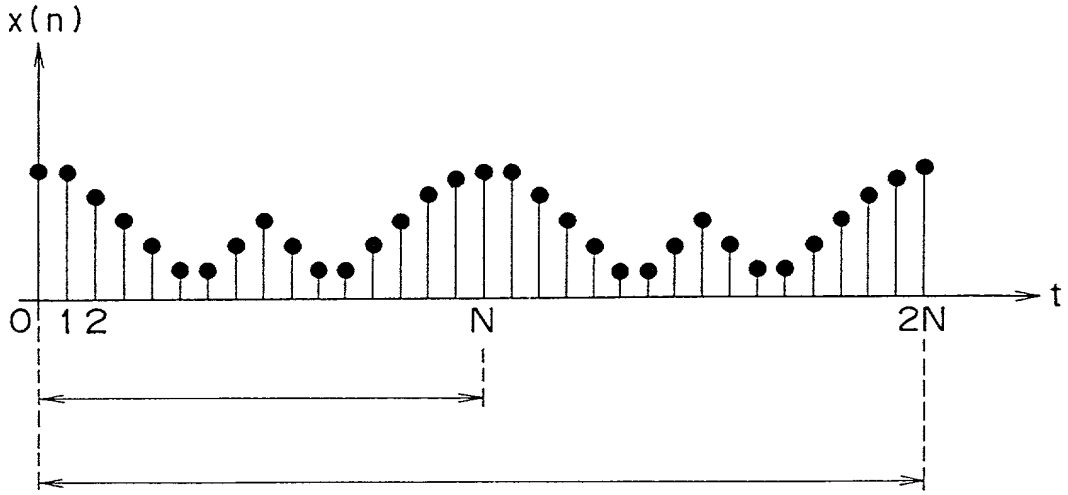


FIG. 79A

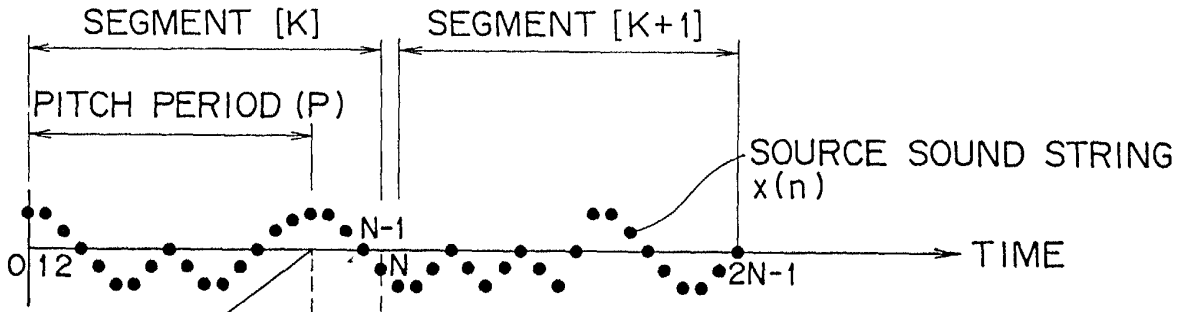


FIG. 79B

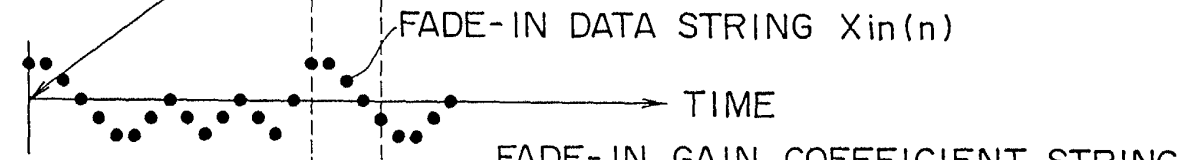


FIG. 79C

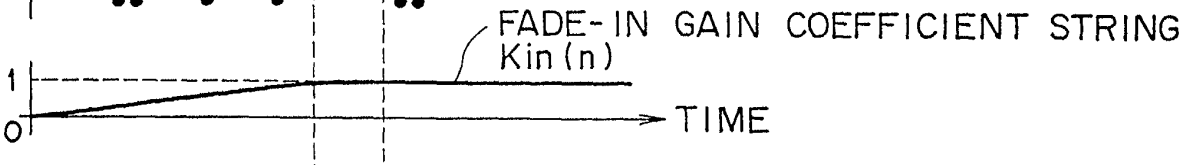


FIG. 79D

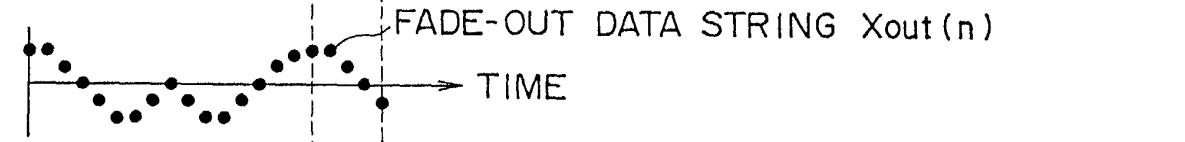


FIG. 79E

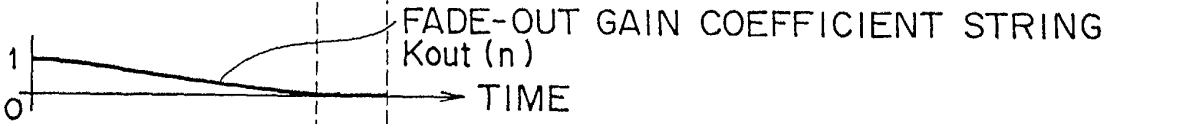


FIG. 79F

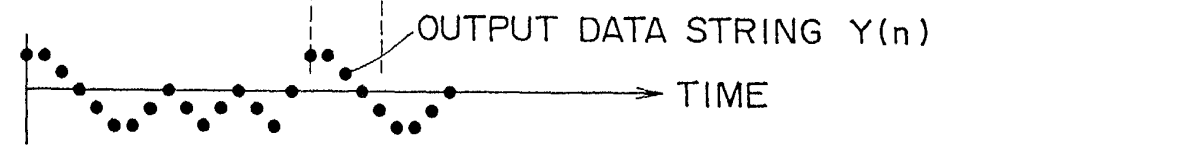


FIG. 80

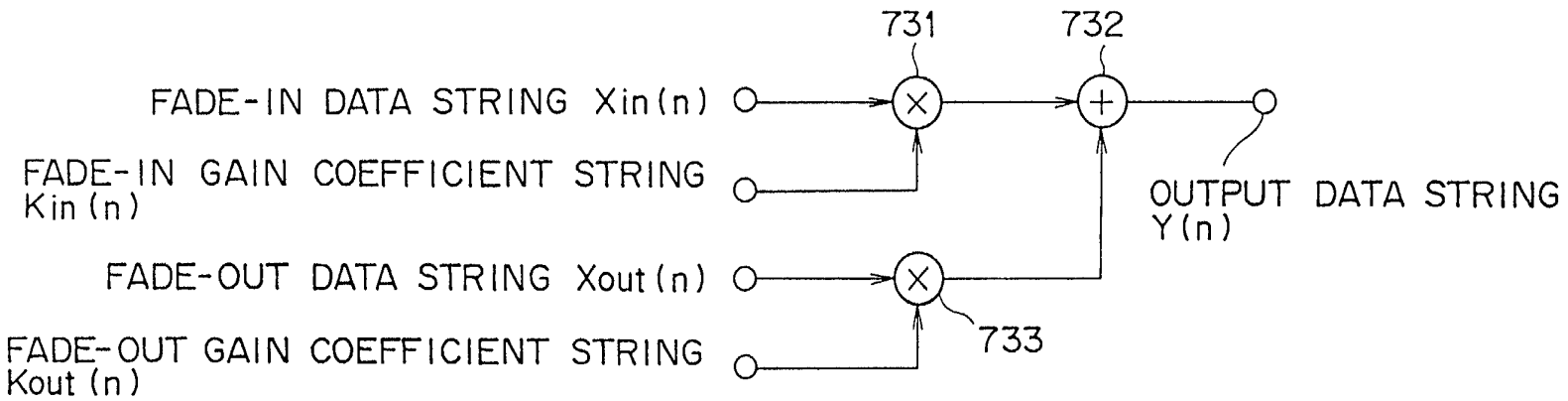

731
732
FADE-IN DATA STRING Xin(n)
FADE-IN GAIN COEFFICIENT STRING Kin(n)
OUTPUT DATA STRING Y(n)
FADE-OUT DATA STRING Xout(n)
733
FADE-OUT GAIN COEFFICIENT STRING Kout(n)

FIG. 81A

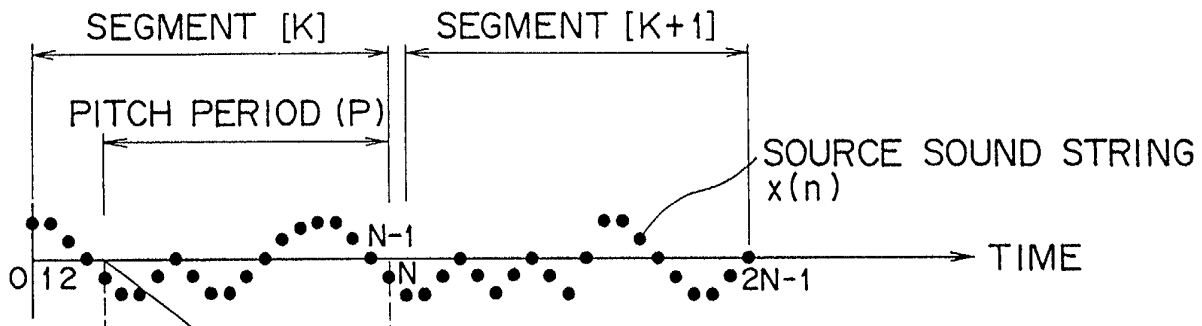


FIG. 81B

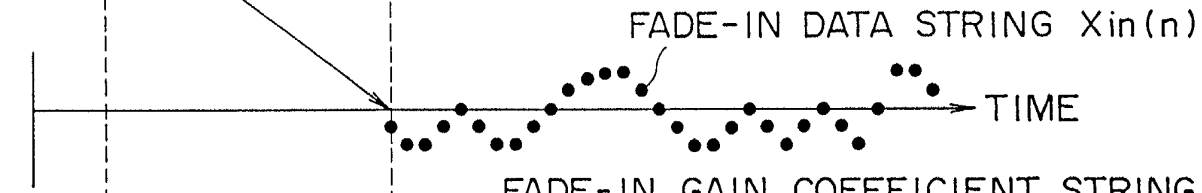


FIG. 81C

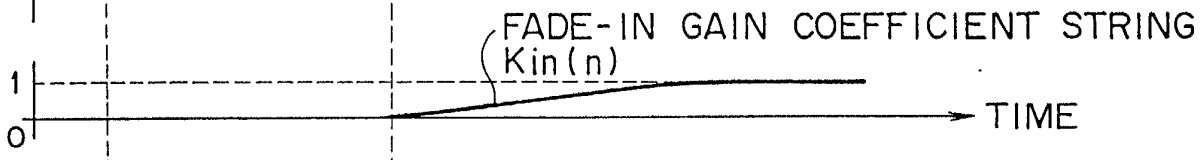


FIG. 81D

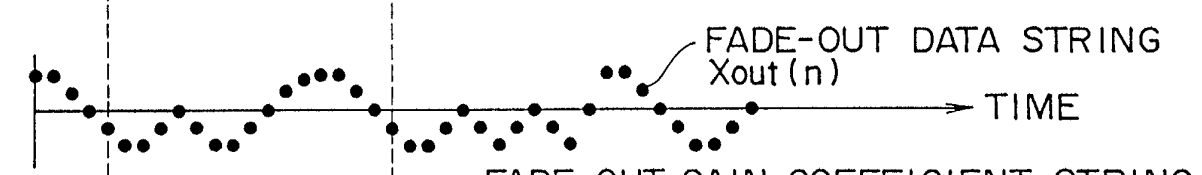


FIG. 81E

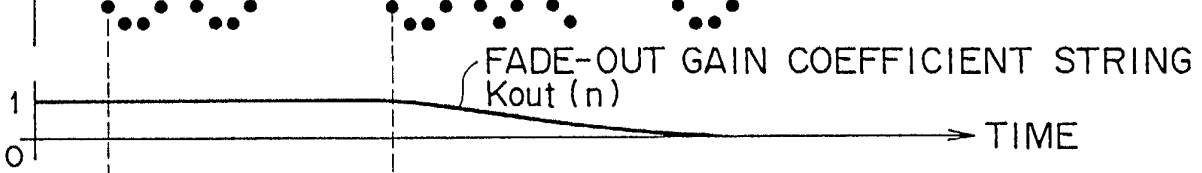


FIG. 81F

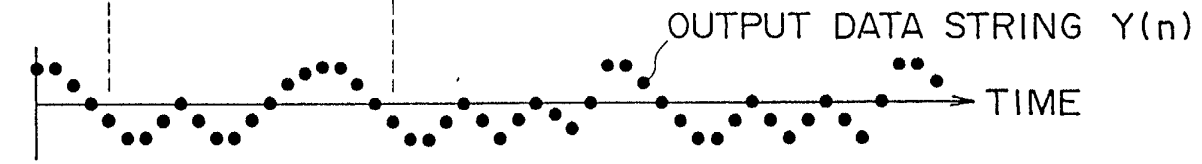


FIG. 82

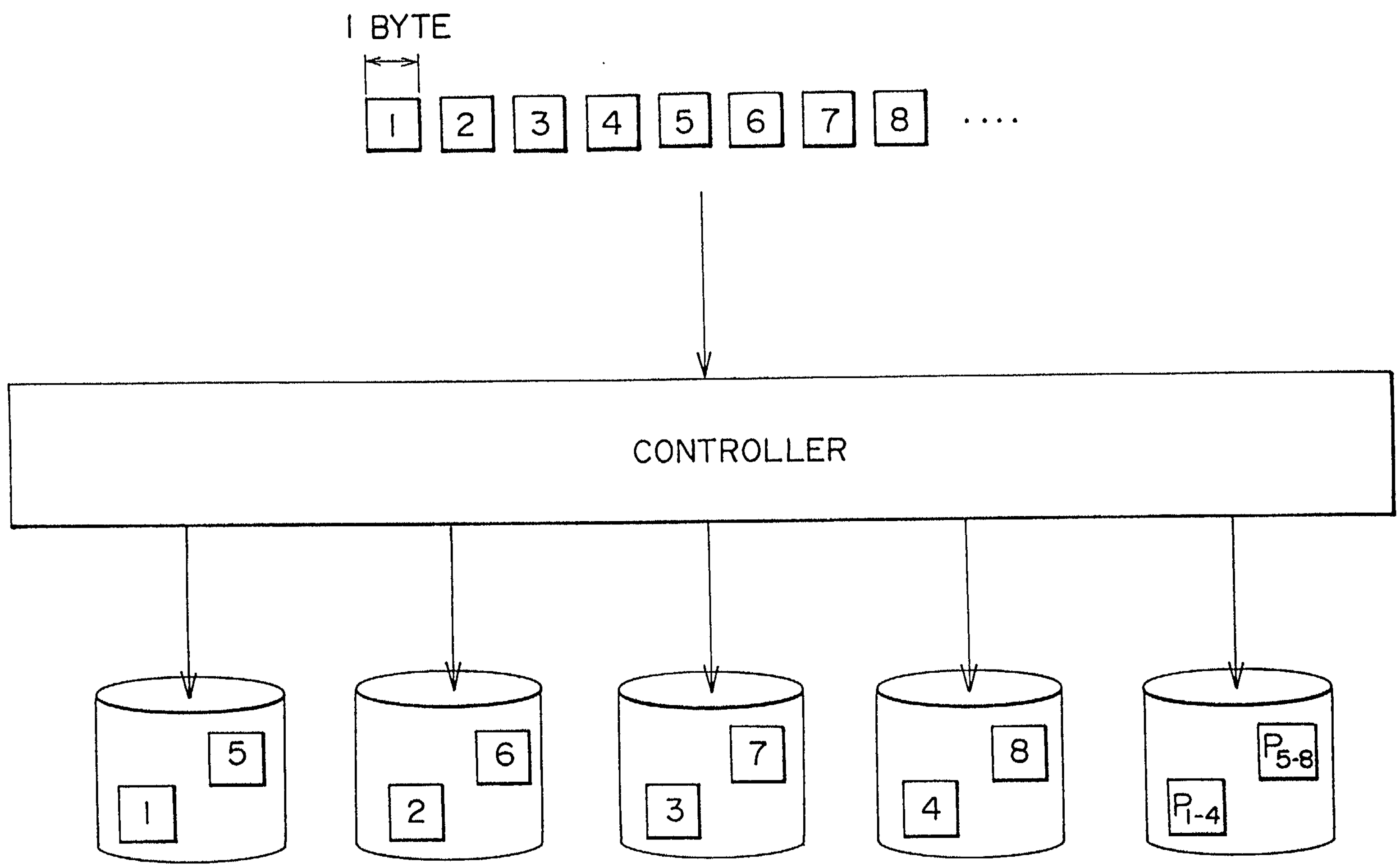


FIG.83